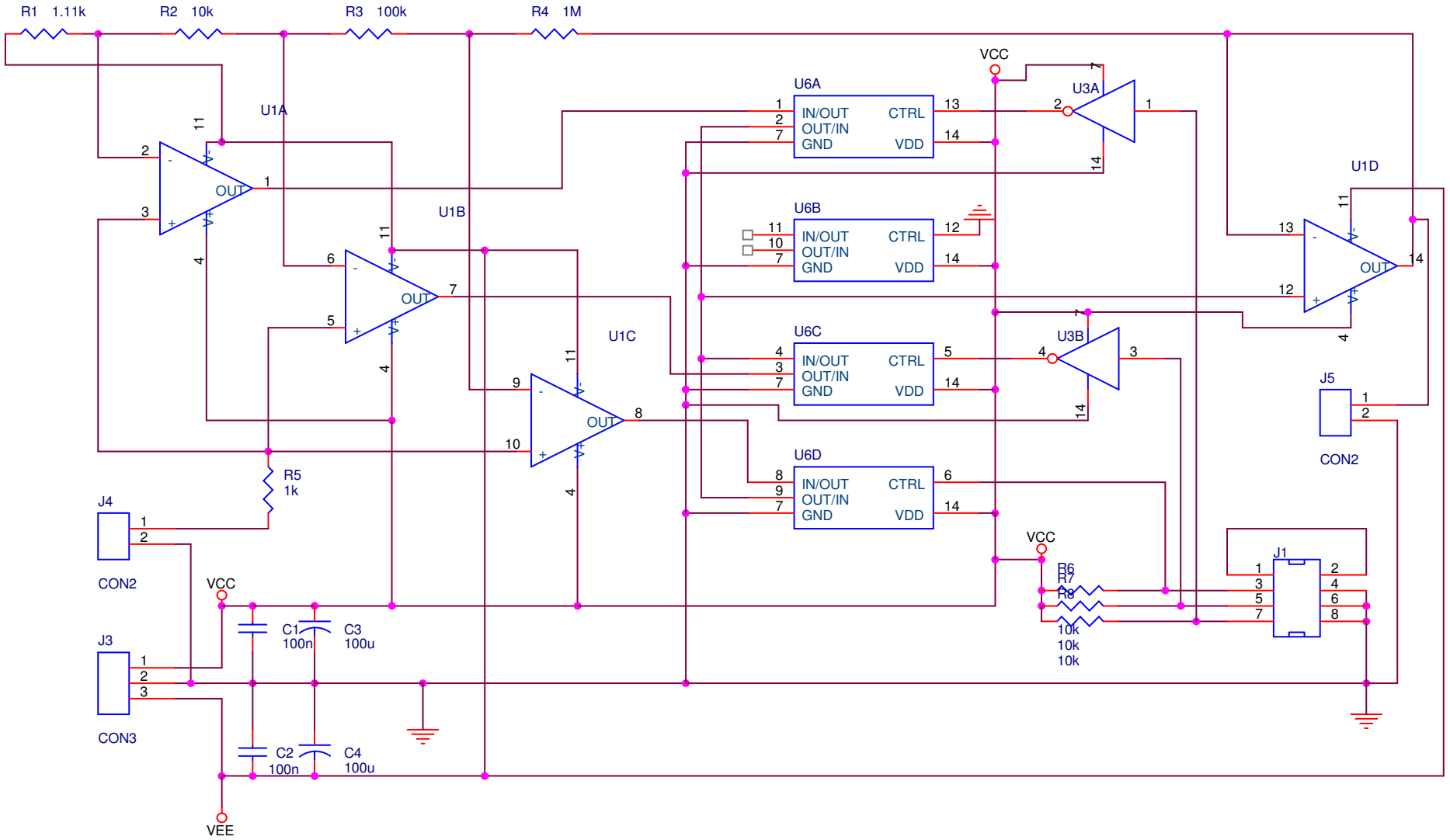
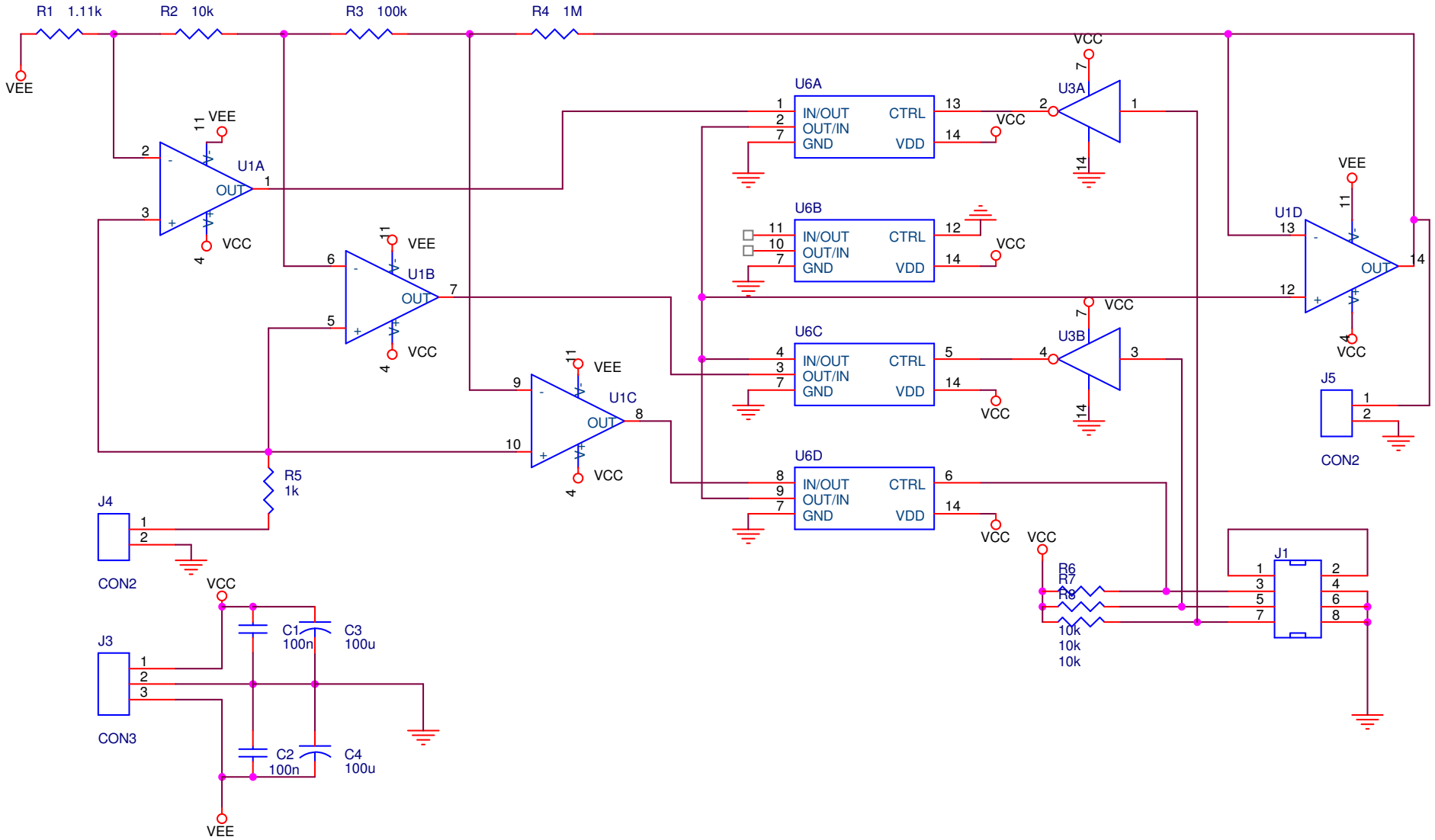
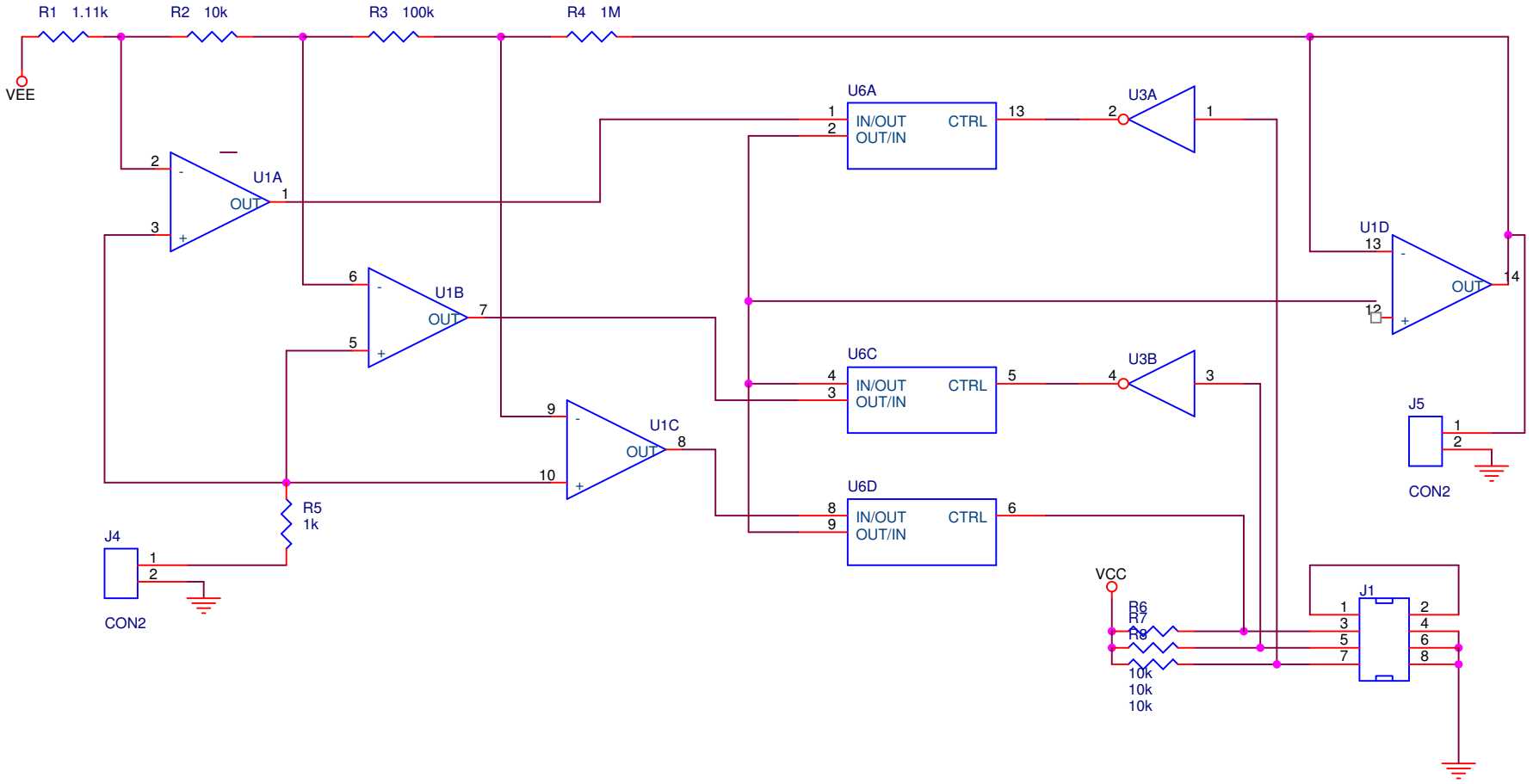
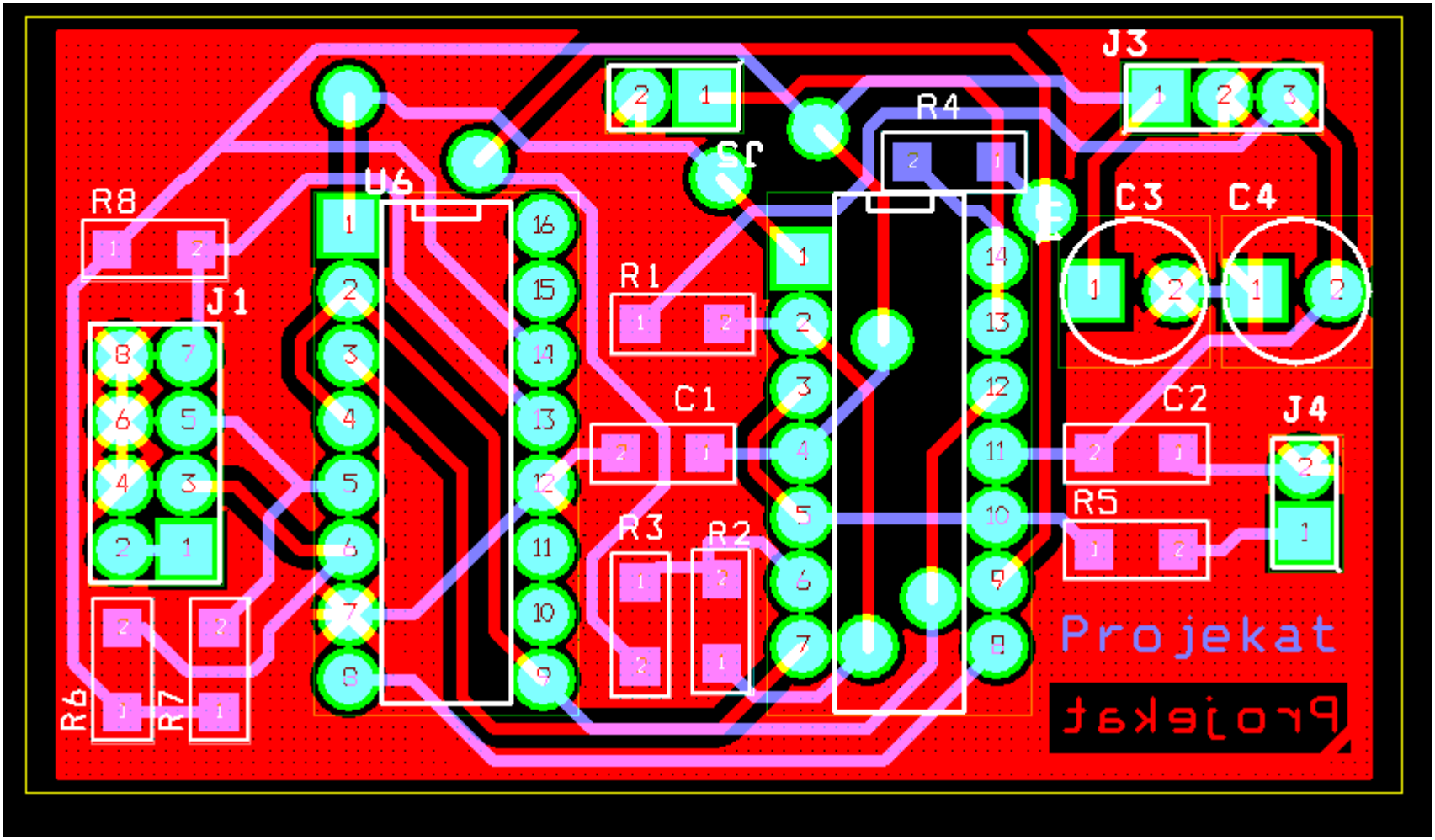
Napajanje u elektronskim kolima

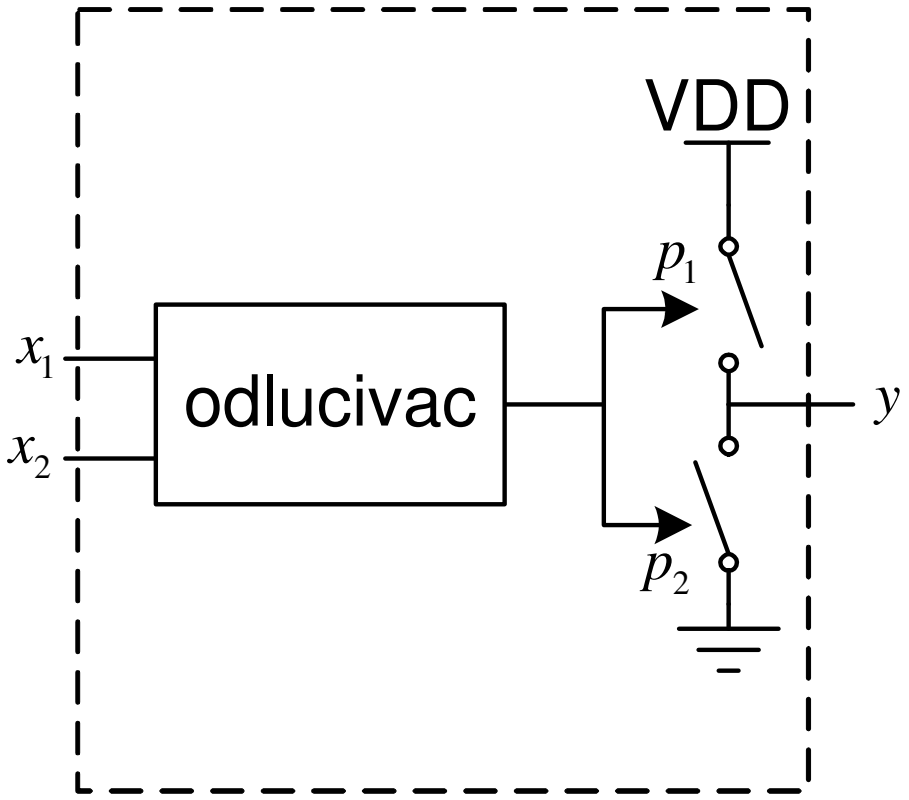



R1 1.11k
R2 10k
R3 100k
R4 1M
VEE
U1A
U1B
U1C
U1D
VCC
U6A
U6B
U6C
U6D
IN/OUT
OUT/IN
GND
CTRL
VDD
U3A
U3B
J1
J3
J4
J5
CON2
CON3
R5
1k
R6
R7
R8
10k
C1
100n
C2
100n
C3
100u
C4
100u


R1 1.11k
R2 10k
R3 100k
R4 1M
VEE
U1A
OUT
U1B
OUT
U1C
OUT
U1D
OUT
U6A
IN/OUT
OUT/IN
CTRL
U6C
IN/OUT
OUT/IN
CTRL
U6D
IN/OUT
OUT/IN
CTRL
U3A
U3B
R5
1k
J4
CON2
J5
CON2
VCC
R6
R7
R8
10k
10k
10k
J1


J3
R4
J5
U6
R8
J1
R1
C1
C3
C4
C2
J4
R5
R3
R2
R6
R7
Projekat

Model idealnog logičkog kola

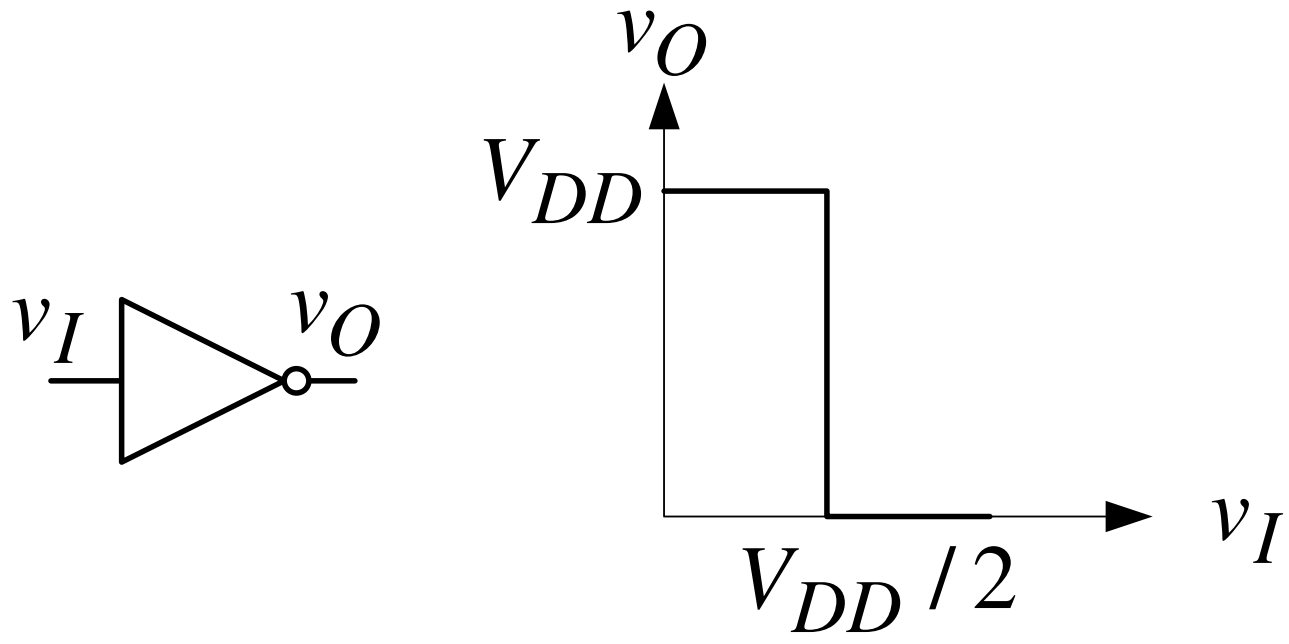


- Funkcije odlučivača: EXOR, XOR, AND, NAND, OR, NOR…
- Prekidači ne smeju istovremeno da budu uključeni, ostale tri kombinacije su dozvoljene → 3 logička stanja!

Statičke karakteristike idealnog logičkog kola

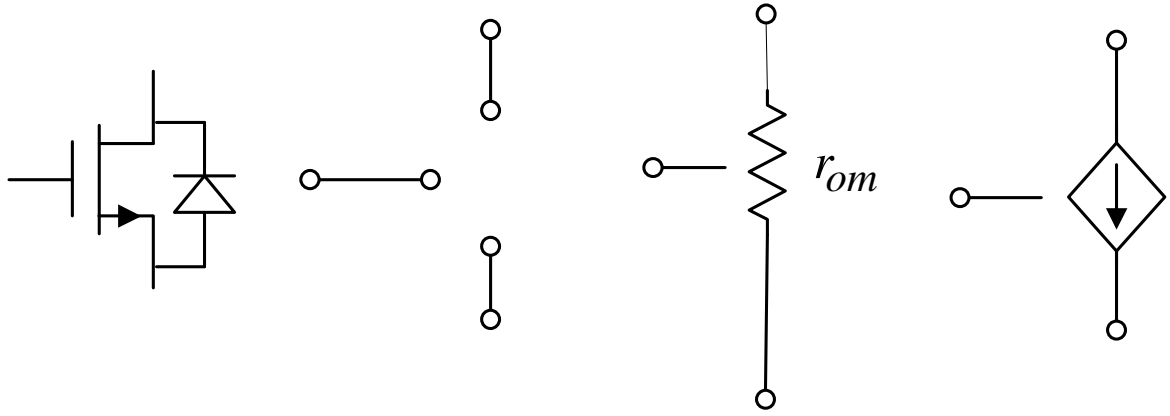
- Pozitivna logika V(1)>V(0)
- *Negativna logika V(1)<V(0)*
- V(1)=V_{DD}
- V(0)=0
- $V_{th}=V_{DD}/2$
- $R_{izl}\rightarrow 0$
- $R_{ul}\rightarrow \infty$

Primer:invertor



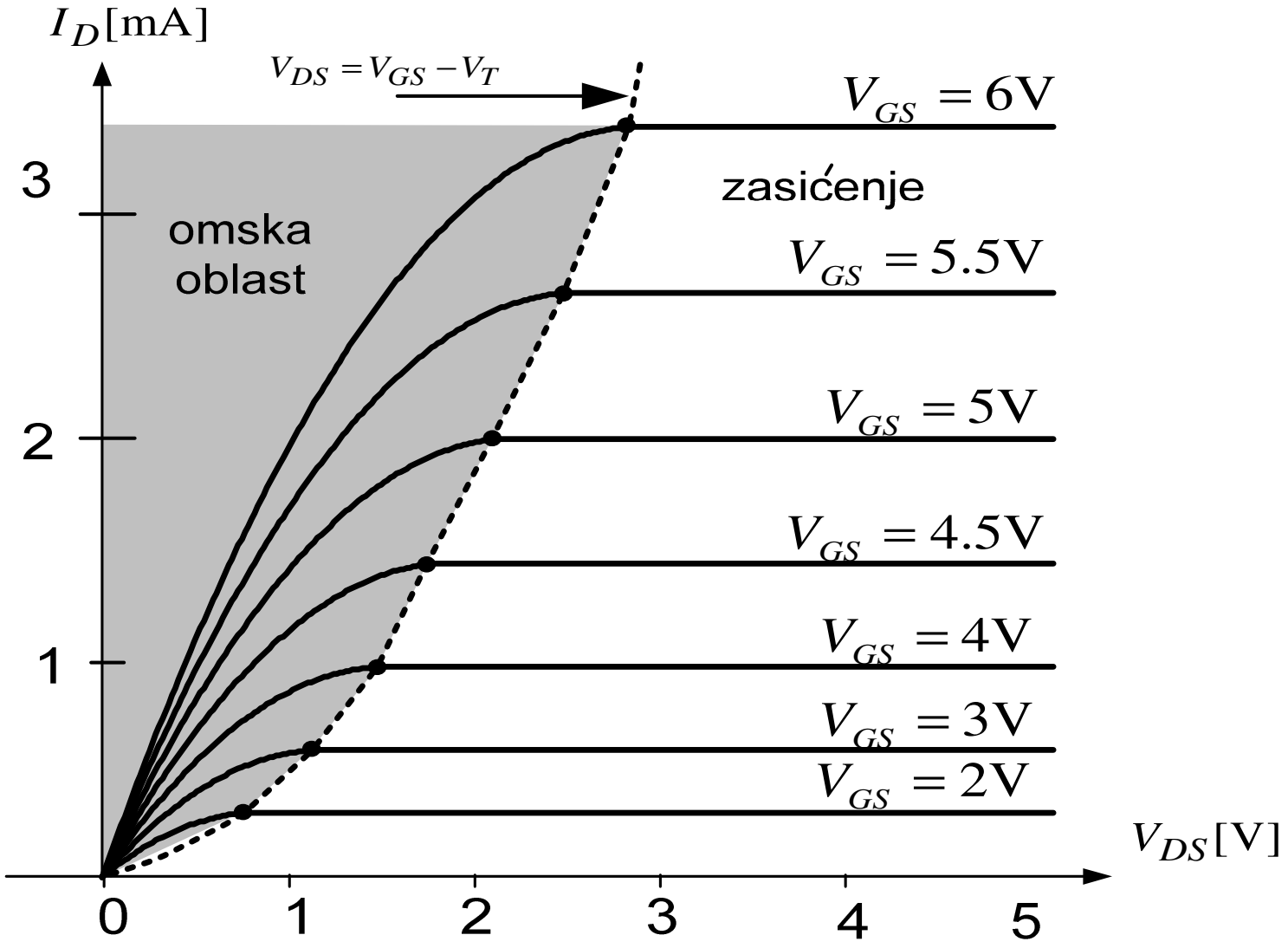
MOS tranzistor kao prekidač

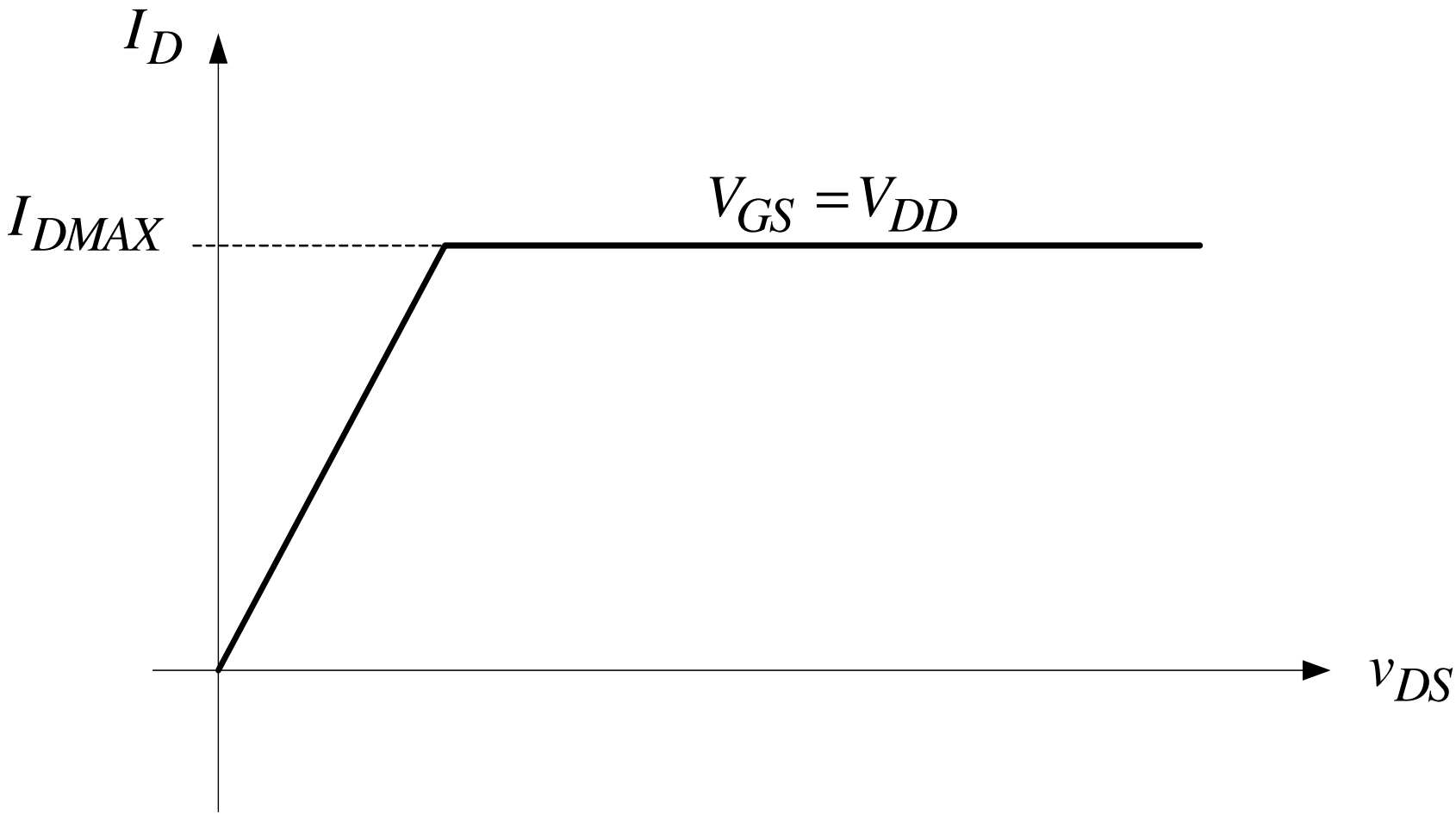
- princip rada



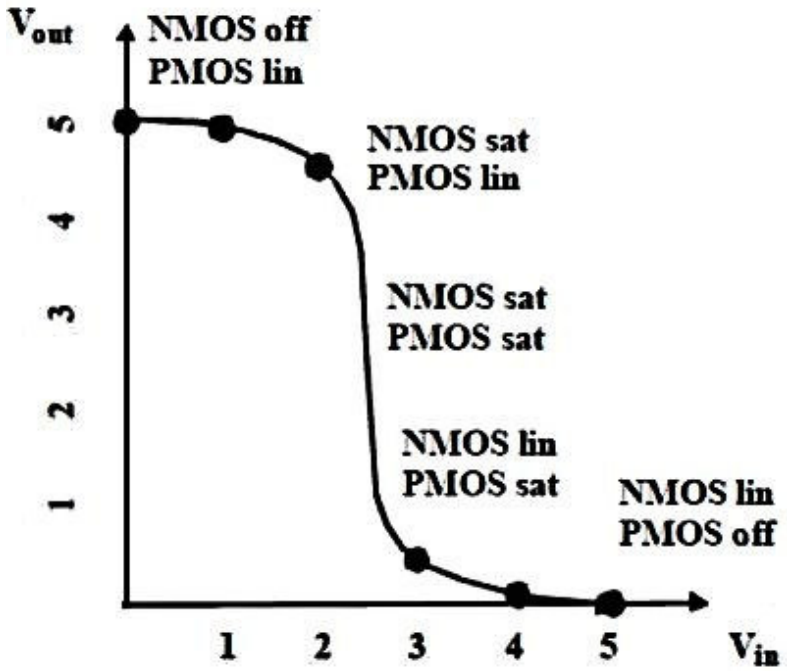
$$I_D = \begin{cases} \approx 0, \quad V_{GS} < \mathrm{V_T} \\ \frac{\mathrm{B}}{2}\left(V_{GS} - \mathrm{V_T}\right)^2 \left(1 + \lambda V_{DS}\right) \approx \frac{\mathrm{B}}{2}\left(V_{GS} - \mathrm{V_T}\right)^2, \quad V_{GS} > \mathrm{V_T}, V_{DS} \geq V_{GS} - \mathrm{V_T} \\ \frac{\mathrm{B}}{2}\left[2\left(V_{GS} - \mathrm{V_T}\right)V_{DS} - {V_{DS}}^2\right], \quad V_{GS} > \mathrm{V_T}, V_{DS} < V_{GS} - \mathrm{V_T} \end{cases}$$

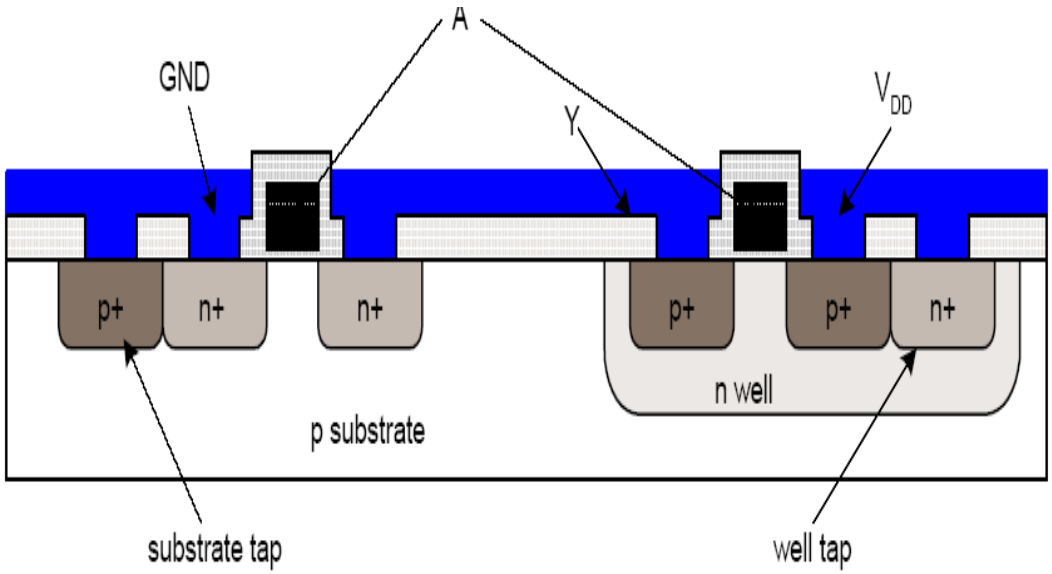
$$I_D = \frac{B}{2}\left[2\left(V_{GS} - V_T\right)V_{DS} - {V_{DS}}^2\right] \approx B\left(V_{DD} - V_T\right)V_{DS} = \frac{V_{DS}}{r_{om}}$$

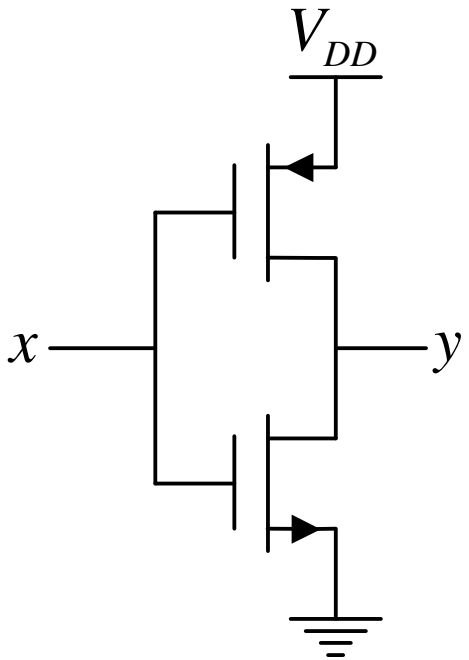

I_D[mA]
$V_{DS} = V_{GS} - V_T$
$V_{GS} = 6$V
zasićenje
omska
oblast
$V_{GS} = 5.5$V
$V_{GS} = 5$V
$V_{GS} = 4.5$V
$V_{GS} = 4$V
$V_{GS} = 3$V
$V_{GS} = 2$V
V_{DS}[V]
3
2
1
0
1
2
3
4
5


I_D
I_{DMAX}
$V_{GS} = V_{DD}$
v_{DS}

Realizacija CMOS invertora



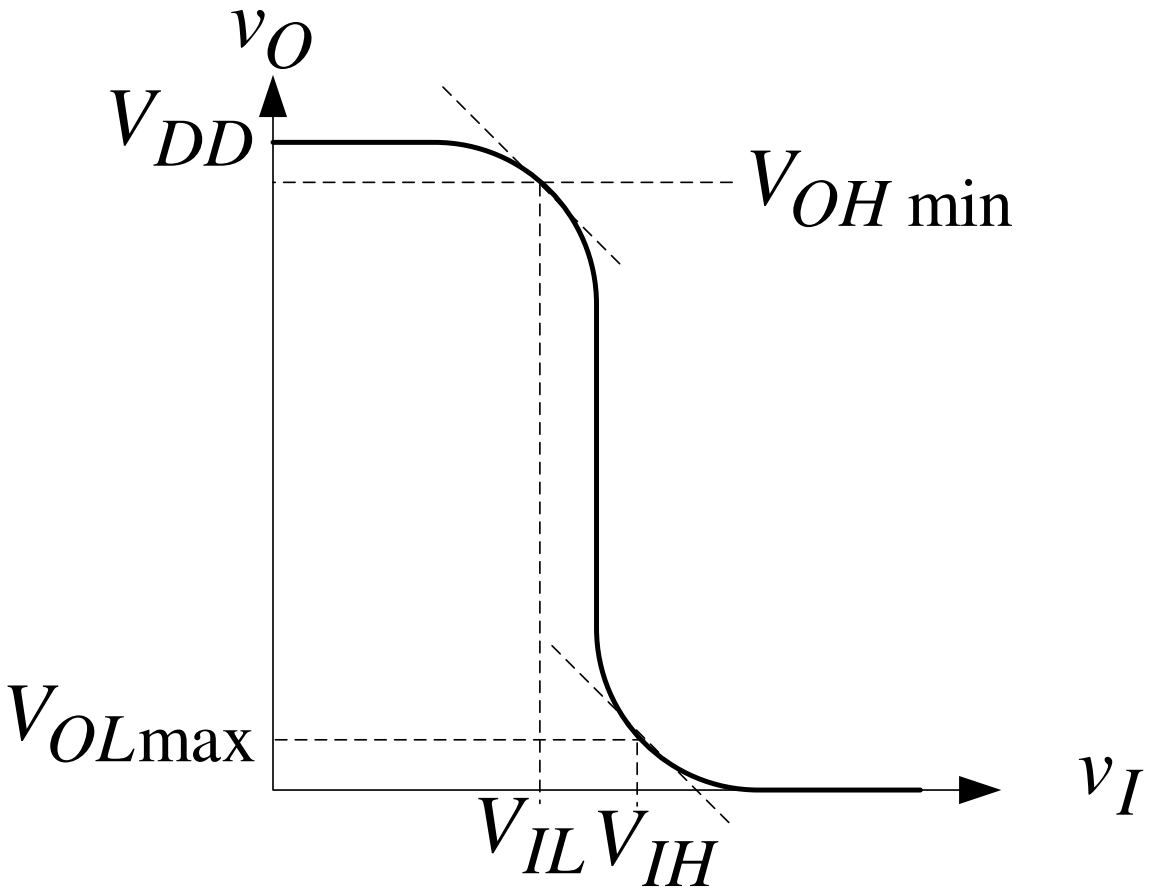




Statičke karakteristike CMOS invertora

- Pozitivna logika V(1)>V(0) √
- $V(1) \neq V_{DD}$! $V(1) = f(I(1))$
- $V(0) \neq 0$! $V(0) = f(I(0))$
- $V_{th} \neq V_{DD}/2$, nema smisla, zabranjena zona!
- $R_{izl} \neq 0$
- $R_{ul} \rightarrow \infty$ √

- V_{OH} –izlazni napon logičke jedinice
- V_{IH} – minimalni napon na ulazu koji kolo prepoznaje kao logičku jedinicu
- V_{OL} –izlazni napon logičke nule
- V_{IL} – maksimalni napon na ulazu koji kolo prepoznaje kao logičku nulu


v_O
V_{DD}
V_{OH} min
V_{OL}max
v_I
V_{IL} V_{IH}

Margine šuma

$V_{OH} - V_{IH}$

$V_{IL} - V_{OL}$

- I_O – izlazna struja
- I_{OH} – maksimalna izlazna struja logičke jedinice
- I_{OL} – maksimalna izlazna struja logičke nule