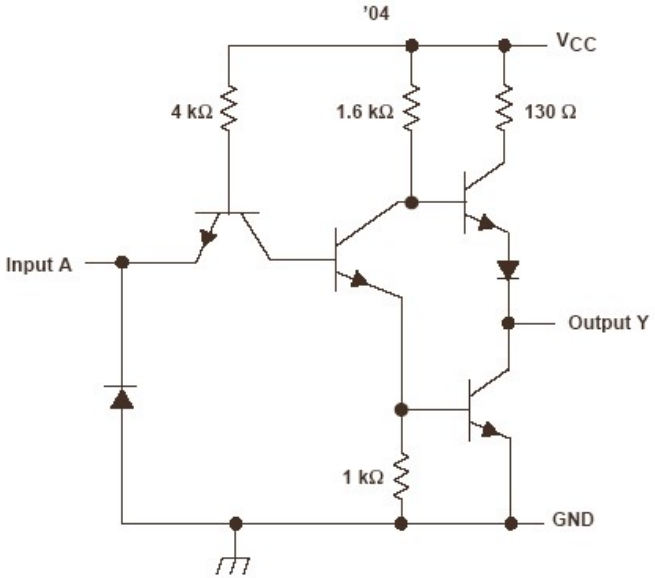
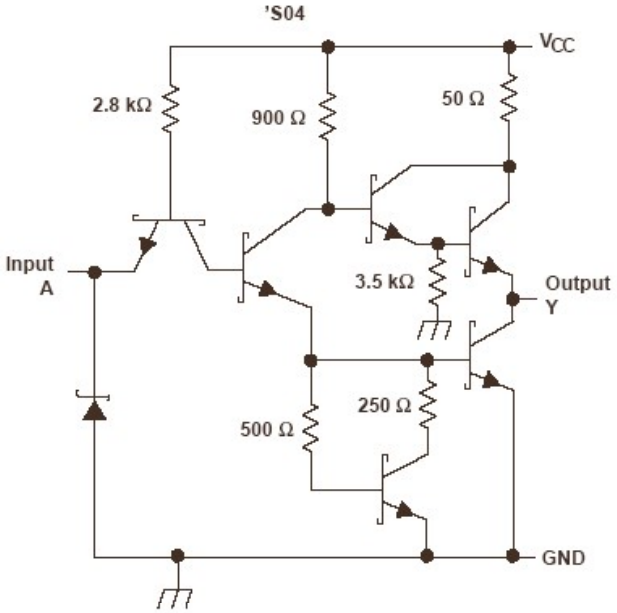
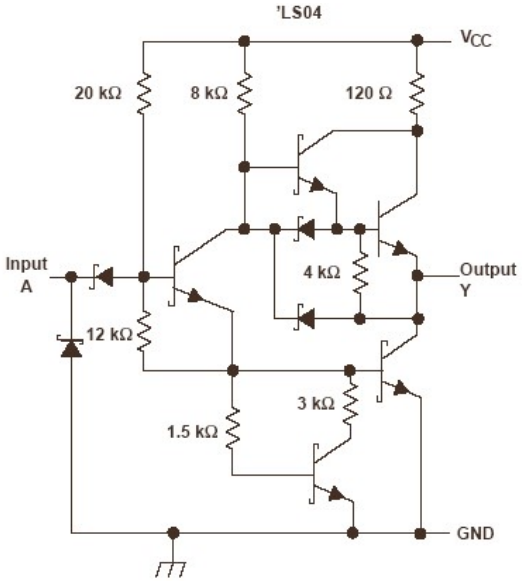
Familije, osobine i realizacija logičkih kola

TTL

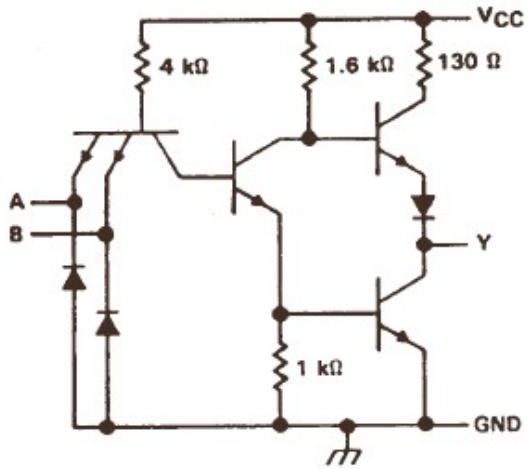
- Kašnjenje u ns
- Standard 10
- LS 10
- ALS 4
- S 3
- F 2


'04
VCC
4 kΩ
1.6 kΩ
130 Ω
Input A
Output Y
1 kΩ
GND

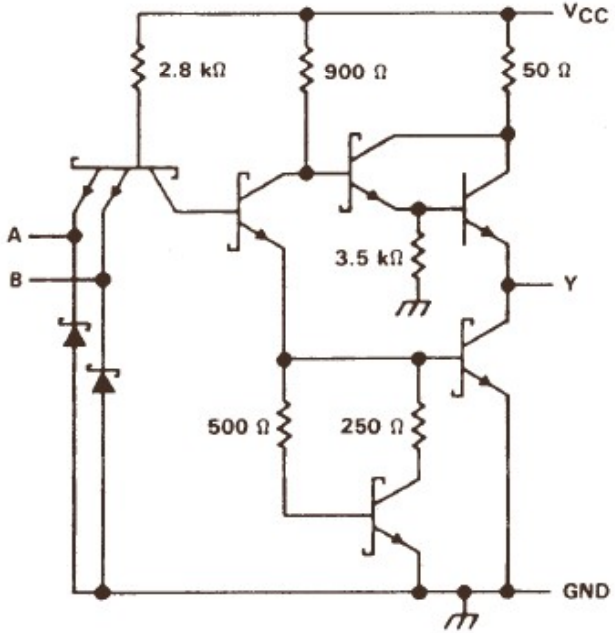

'S04
VCC
2.8 kΩ
900 Ω
50 Ω
Input
A
3.5 kΩ
Output
Y
250 Ω
500 Ω
GND


'LS04
VCC
20 kΩ
8 kΩ
120 Ω
Input
A
4 kΩ
Output
Y
12 kΩ
3 kΩ
1.5 kΩ
GND

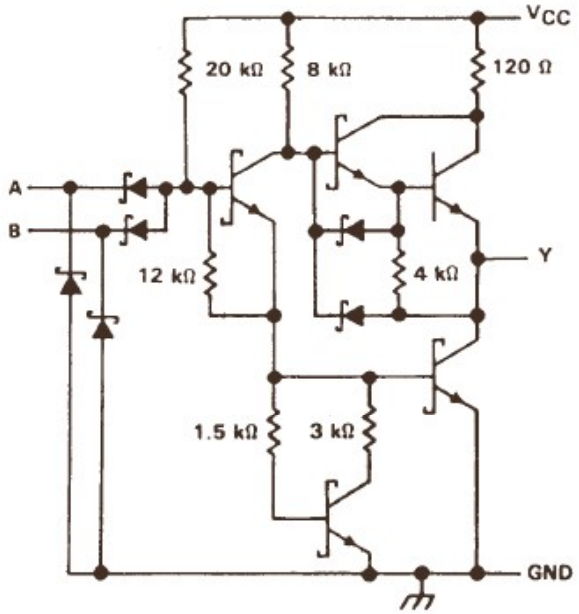
'00


VCC
4 kΩ
1.6 kΩ
130 Ω
A
B
Y
1 kΩ
GND

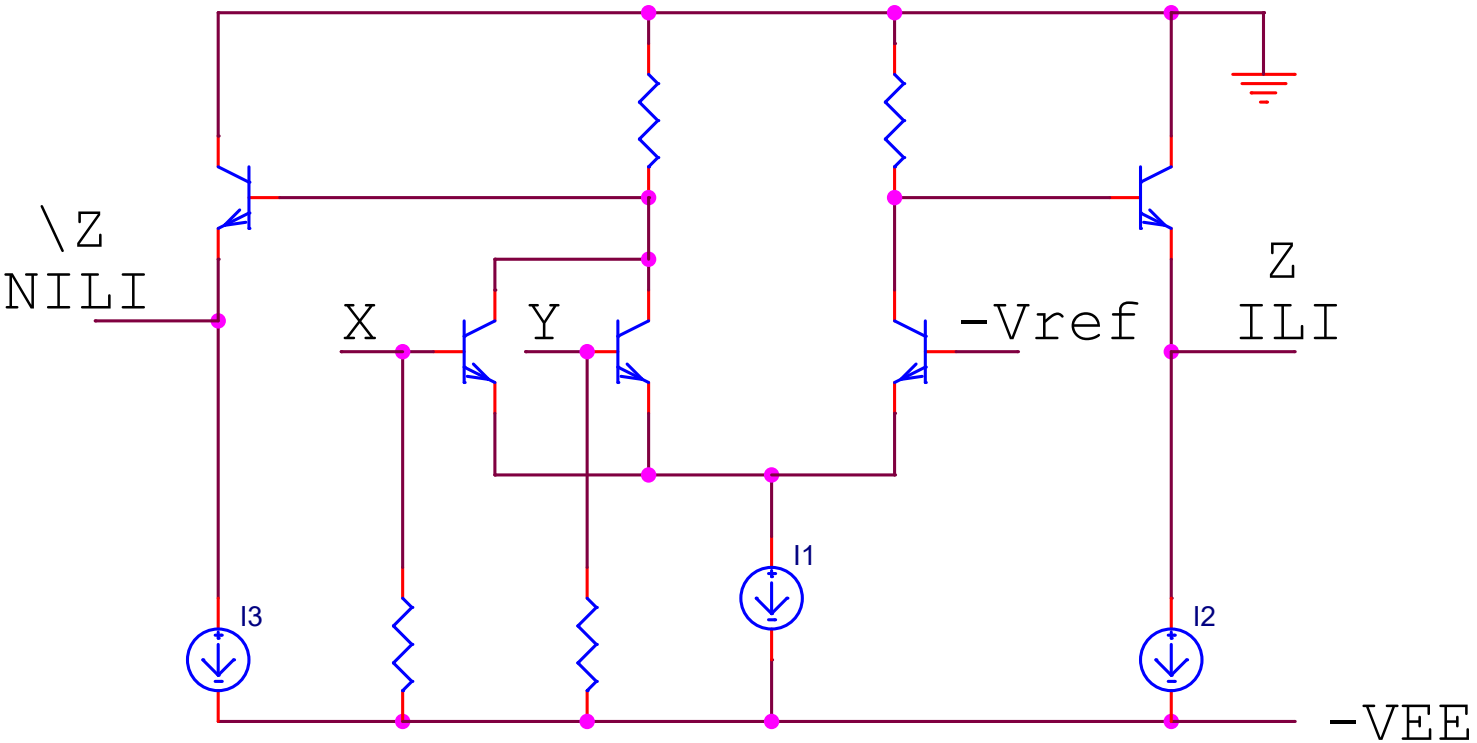
'S00

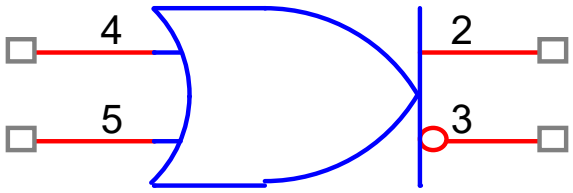

VCC
2.8 kΩ
900 Ω
50 Ω
A
B
3.5 kΩ
Y
500 Ω
250 Ω
GND

'LS00


VCC
20 kΩ
8 kΩ
120 Ω
A
B
12 kΩ
4 kΩ
Y
1.5 kΩ
3 kΩ
GND

ECL





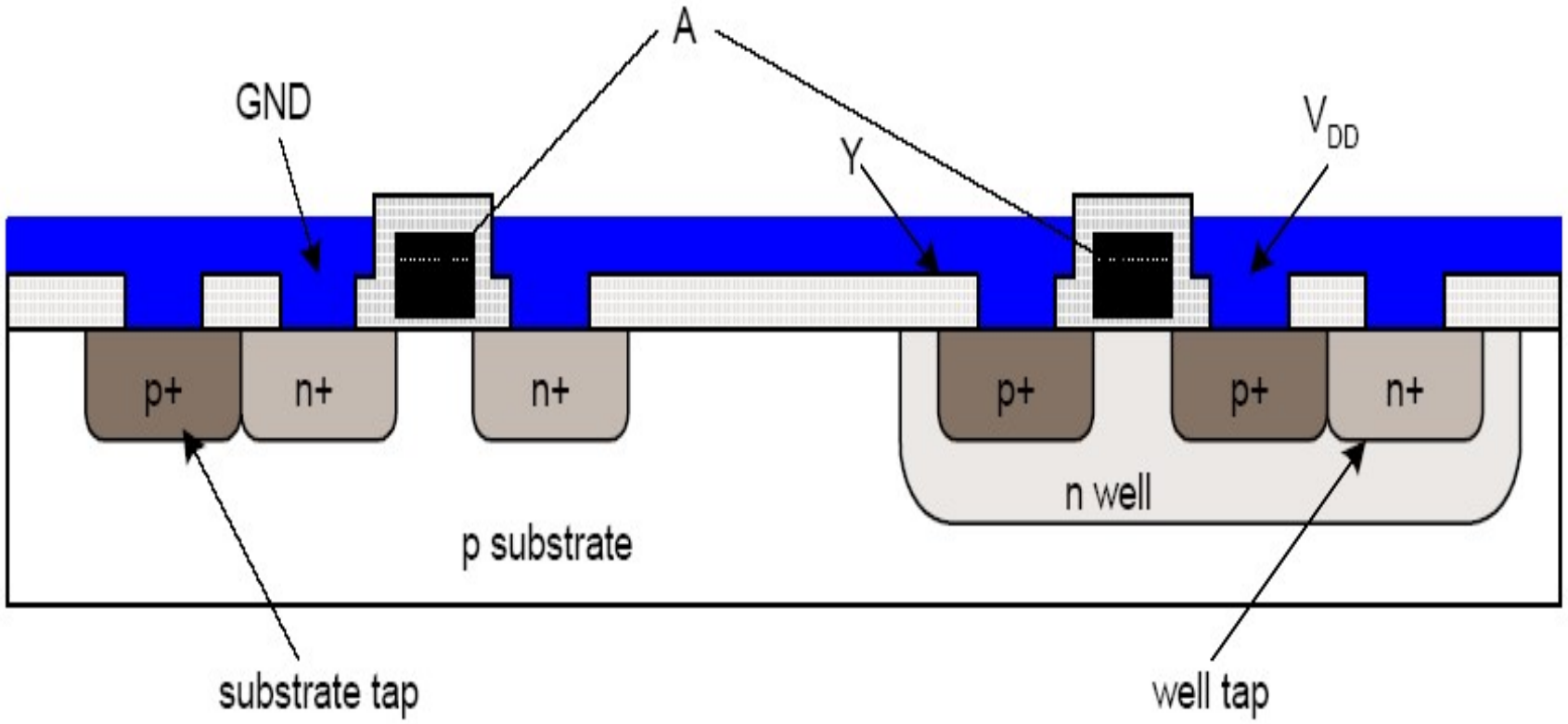
MEC I 8nS
MEC II 2nS
MEC III (16XX) 1nS
101xx 100 series 10K ECL, 3.5nS
102xx 200 series 10K ECL, 2.5nS
108xx 800 series 10K ECL, voltage compensated, 3.5nS
10Hxxx 10K - High speed, voltage compensated, 1.8nS
10Exxx 10K - ECLinPS, voltage compensated, 800pS
100xxx 100K, temperature compensated
100Hxxx 100K - High speed,temperature compensated
100Exxx 100K - ECLinPS, temp, voltage comp., 800pS

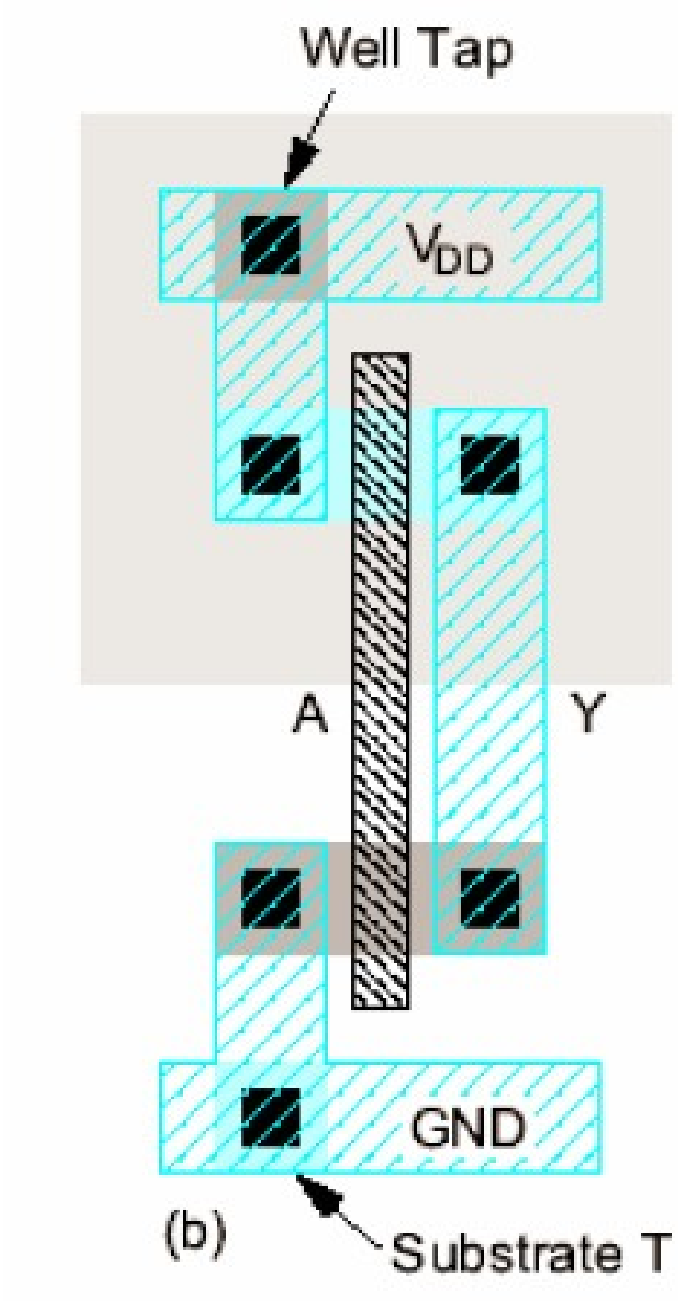
Integrisano 150ps

- Potrošnja skoro da ne zavisi od prekidanja
- 25 x brži od najbržeg CMOS-a
- Niska integracija
- Može GaAs
- Primena – ALU superkompjutera

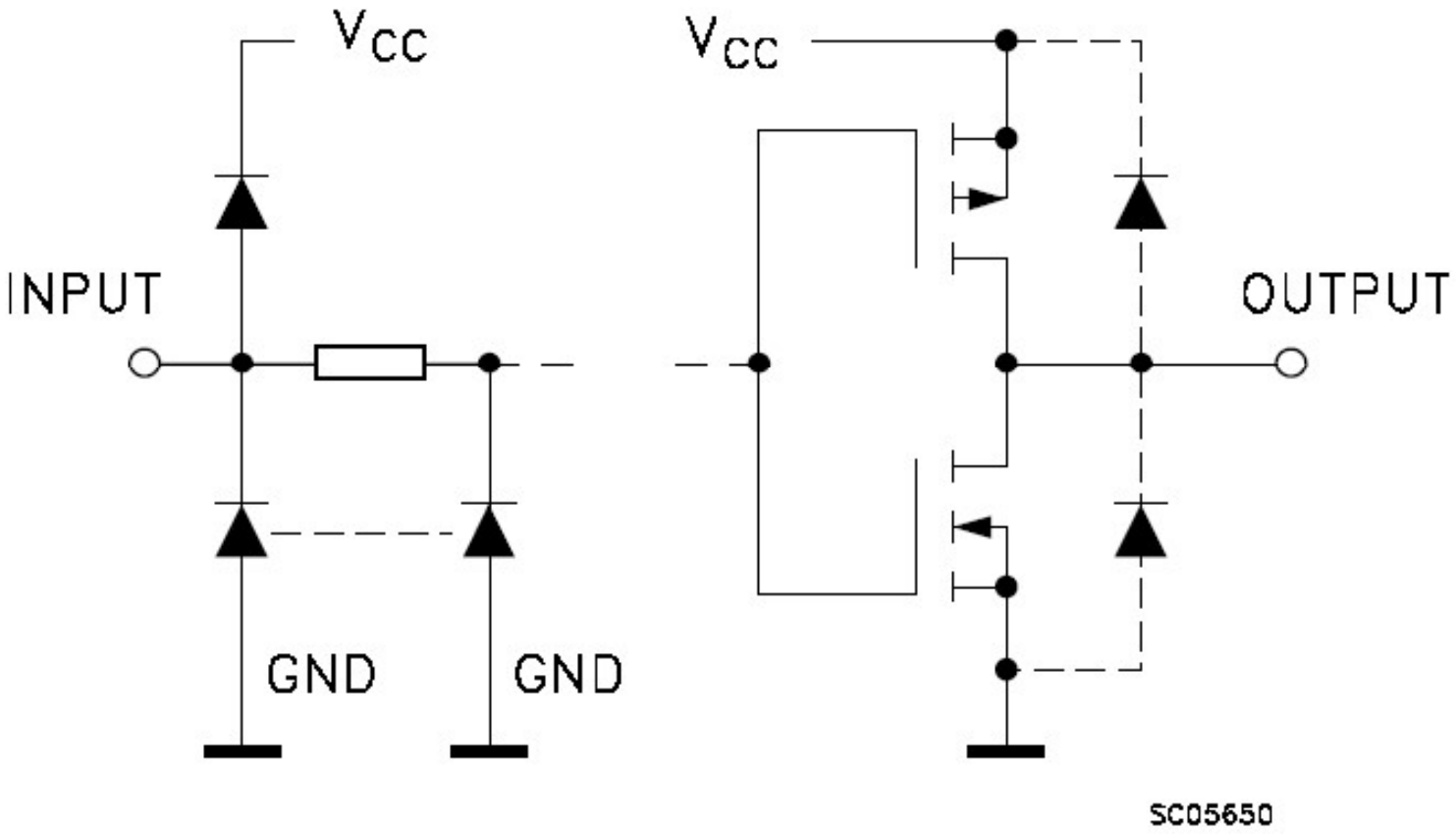
Realizacija logičkih kola u CMOS tehnologiji

Fizička realizacija CMOS invertora

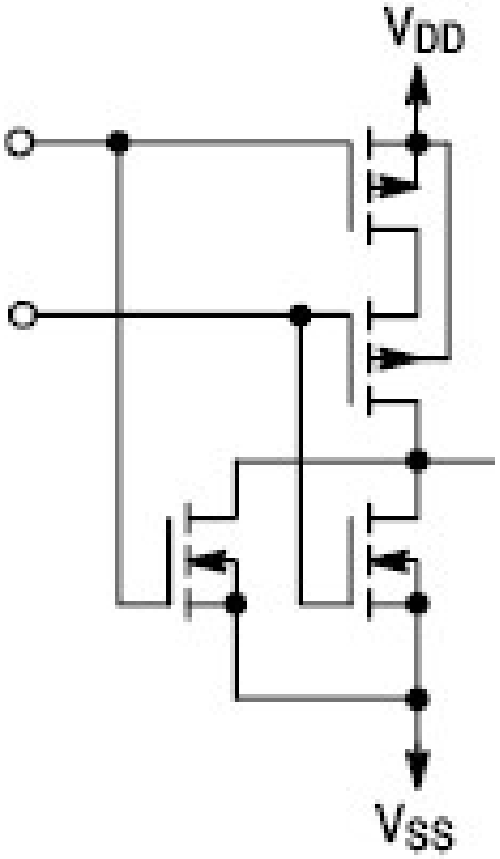



Well Tap
V_{DD}
A
Y
GND
(b)
Substrate T

Zaštita

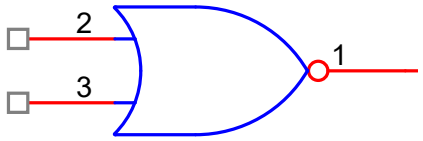


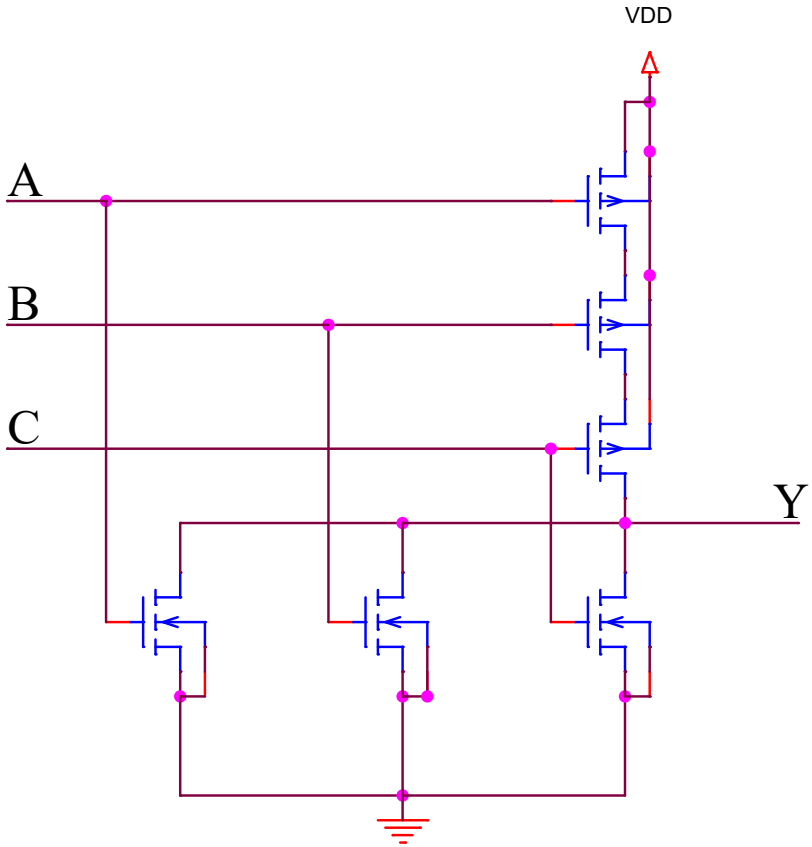
NEBAFERISAN NILI

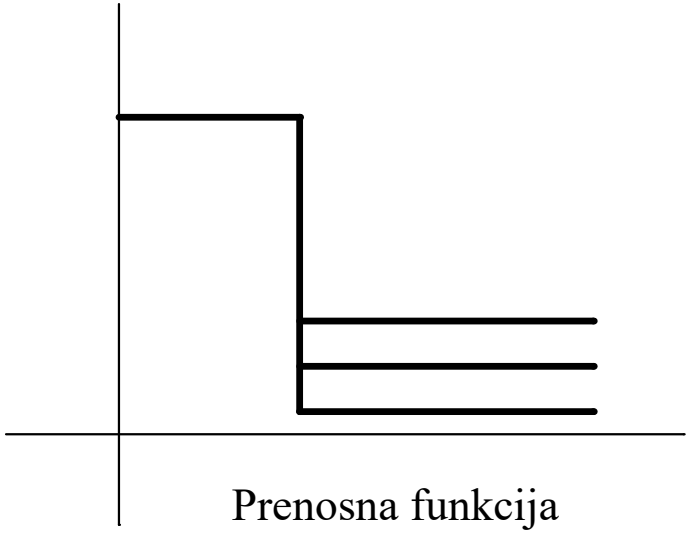


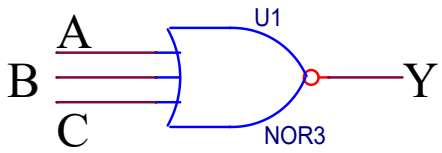
Moraju na ulazima da budu obe nule da bi na izlazu bila jedinica

$$\overline{X} \cdot \overline{Y} = Z = \overline{\overline{X} \cdot \overline{Y}} = \overline{X + Y}$$




VDD
A
B
C
Y

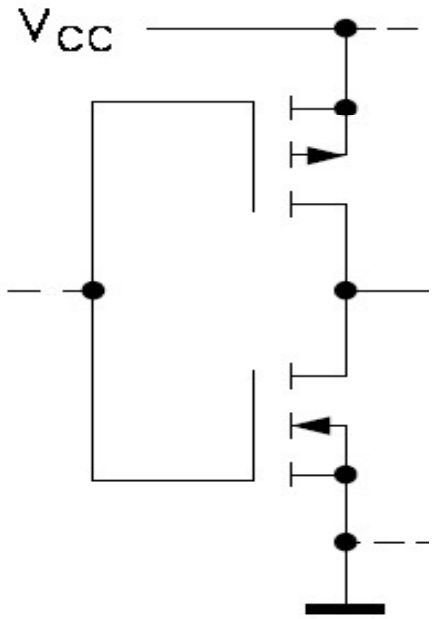

Prenosna funkcija

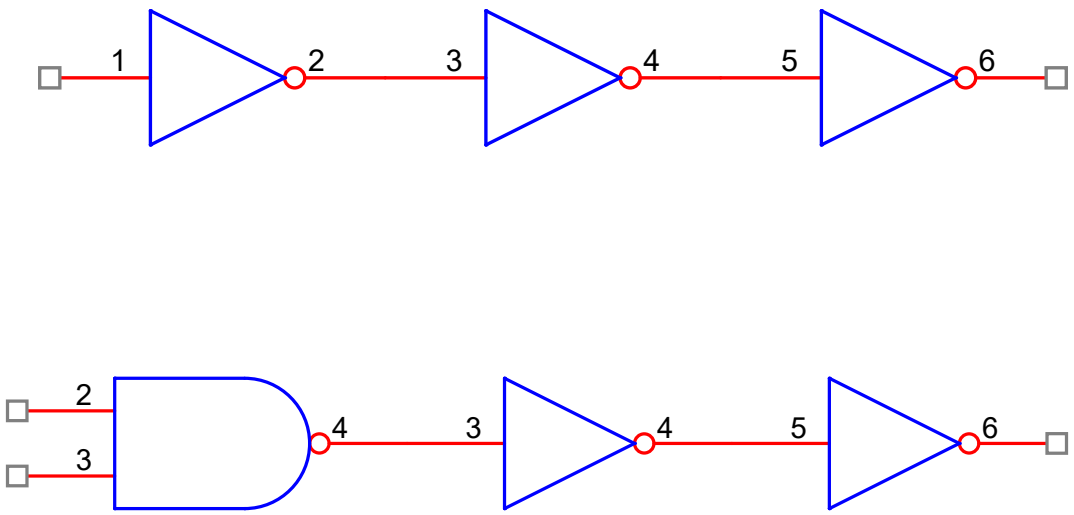

A
B
C
U1
Y
NOR3

Dvostruko baferisanje

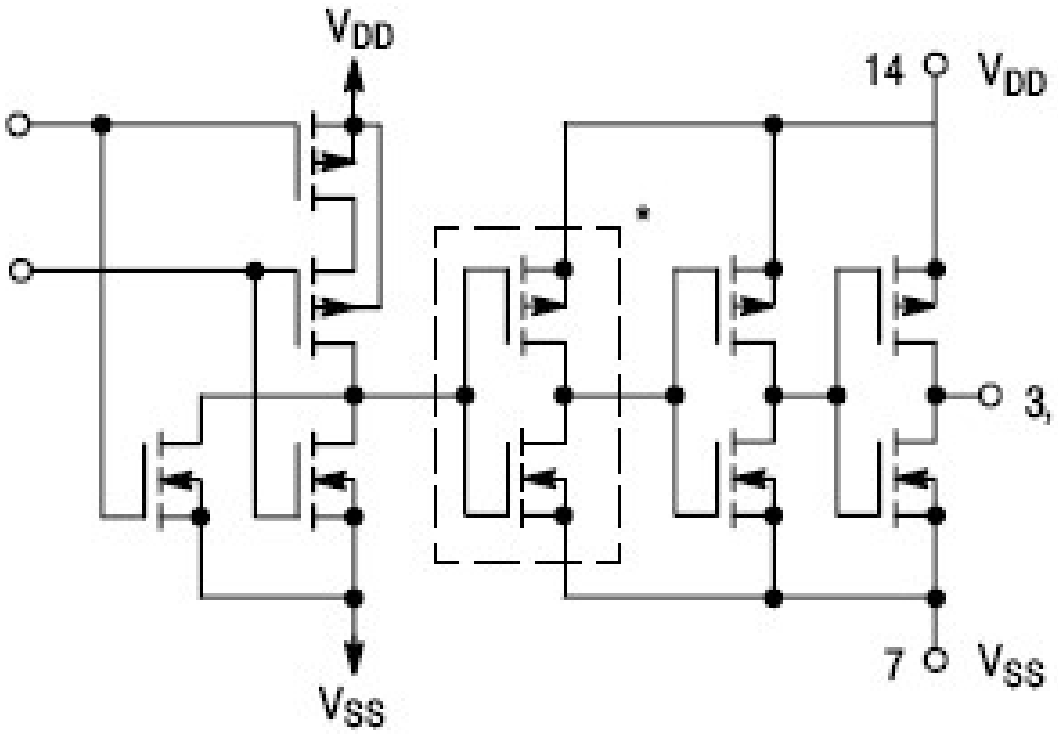
$$I_D = \frac{B}{2}\left[2\left(V_{GS} - V_T\right)V_{DS} - {V_{DS}}^2\right] \approx B\left(V_{DD} - V_T\right)V_{DS} = \frac{V_{DS}}{r_{om}}$$

$$B = \mu C_{ox}\frac{W}{L}$$

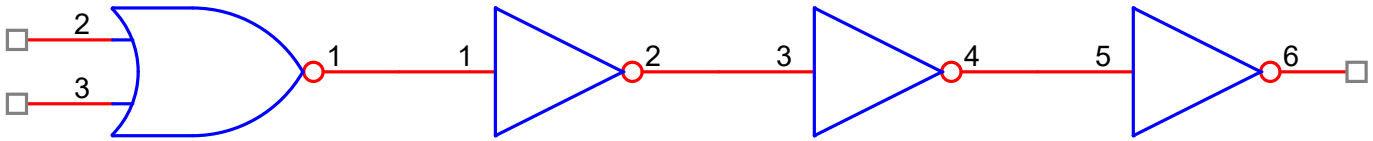


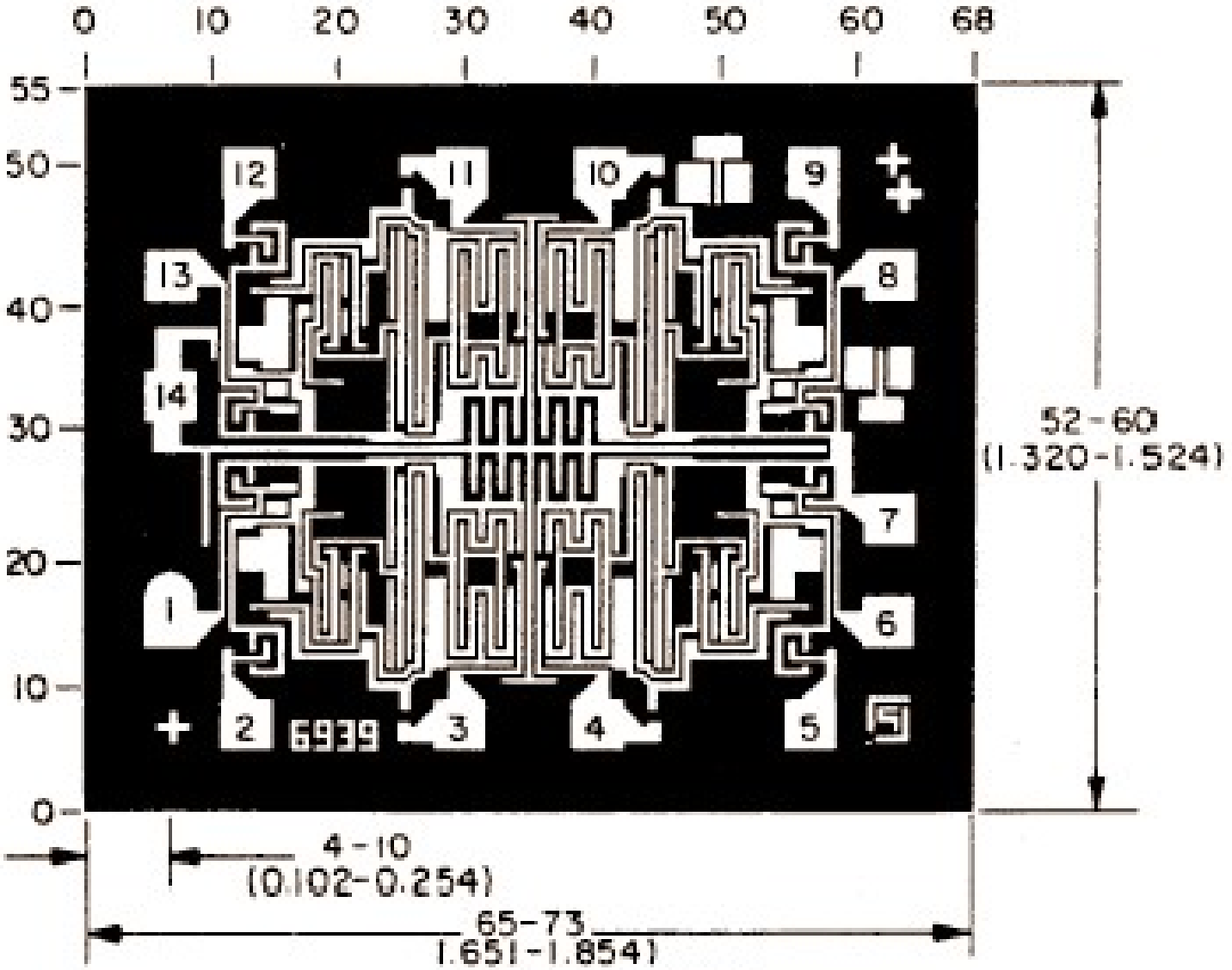

1
2
3
4
5
6
2
3
4
3
4
5
6

NILI i ILI

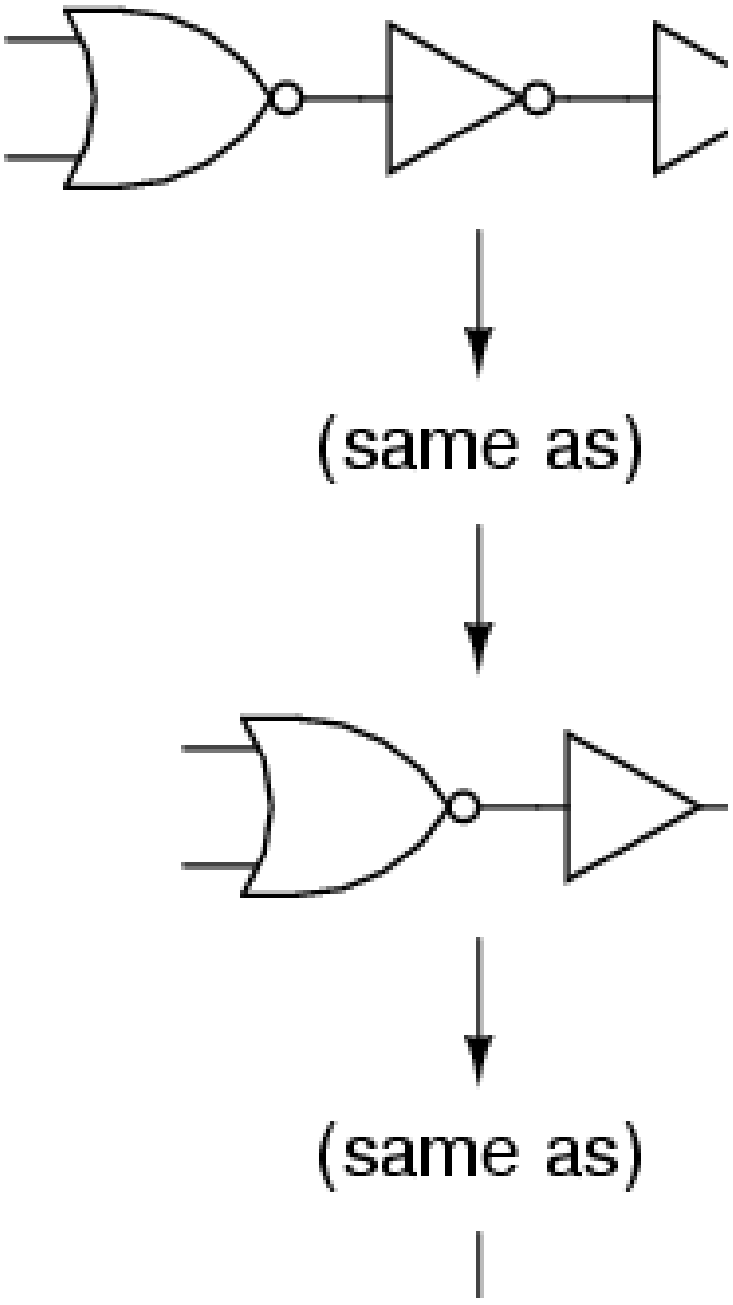


*Inverter omitted in MC14001B

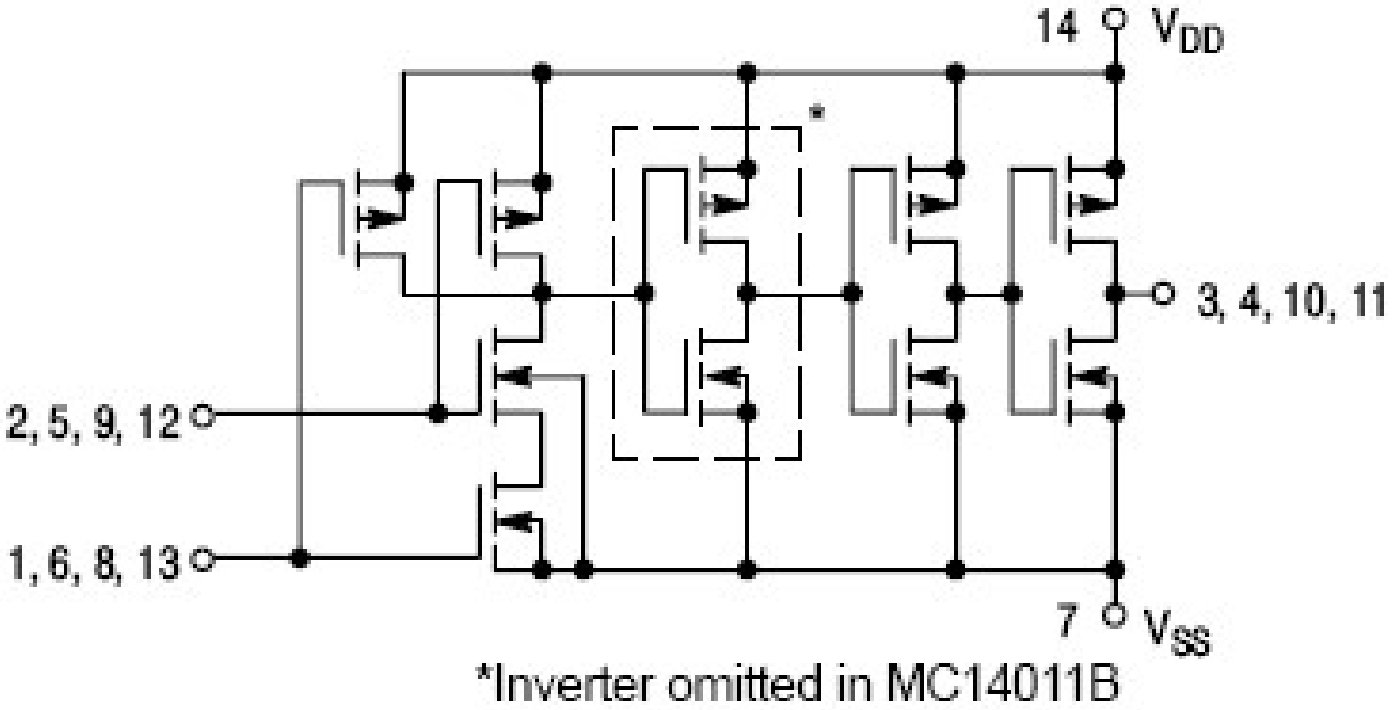


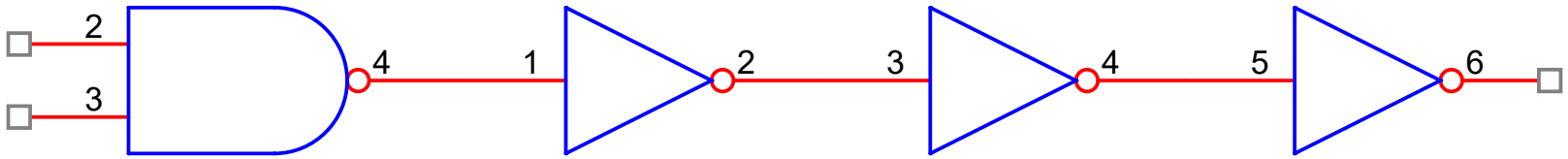

0
10
20
30
40
50
60
68
55
50
40
30
20
10
0
12
11
10
9
13
8
14
7
1
6
2
6939
3
4
5
52-60
(1.320-1.524)
4-10
(0.102-0.254)
65-73
(1.651-1.854)

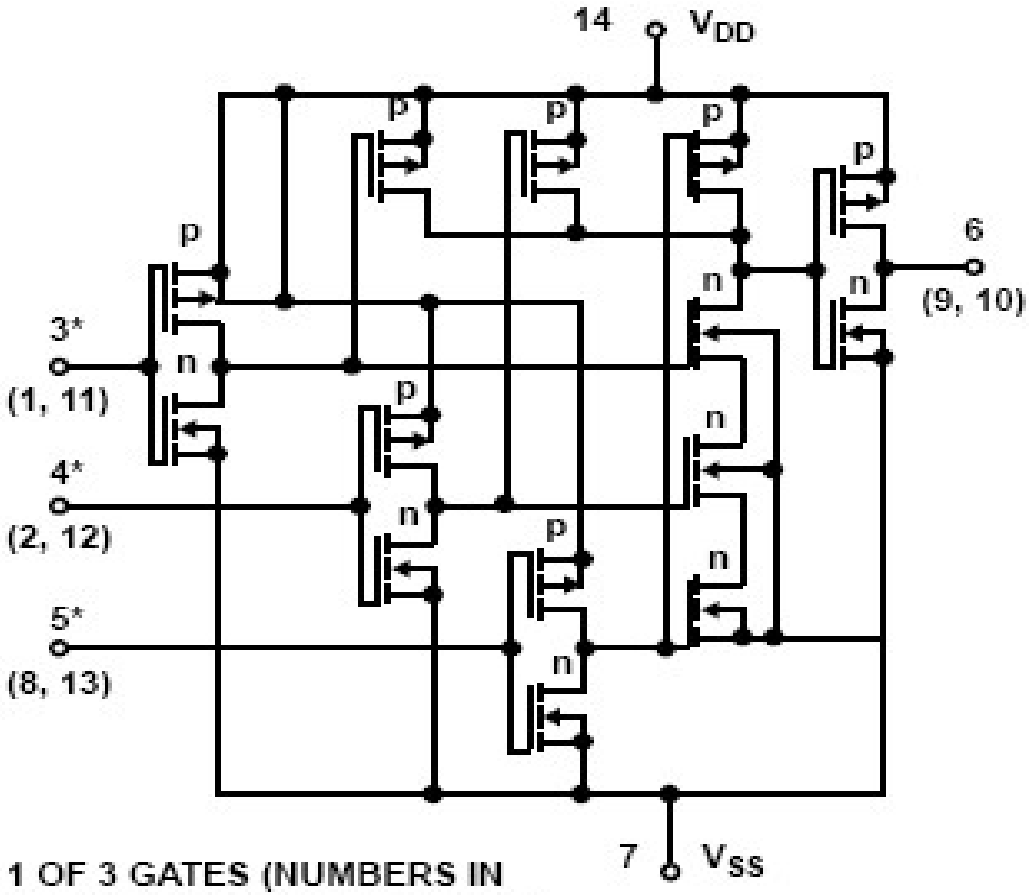
CD4001BMS


(same as)
(same as)

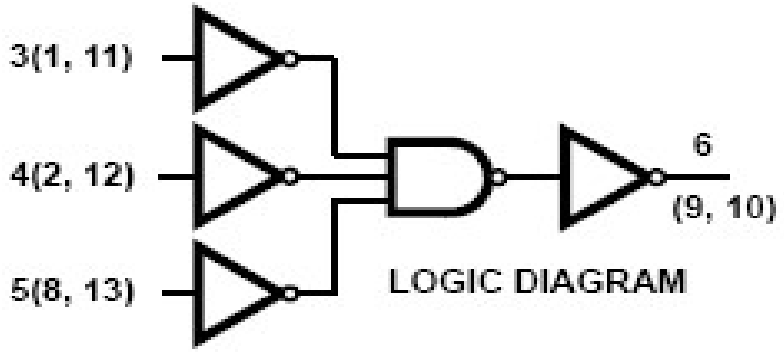
NI i I


14
V_{DD}
3, 4, 10, 11
2, 5, 9, 12
1, 6, 8, 13
7
V_{SS}
*Inverter omitted in MC14011B


2
3
4
1
2
3
4
5
6



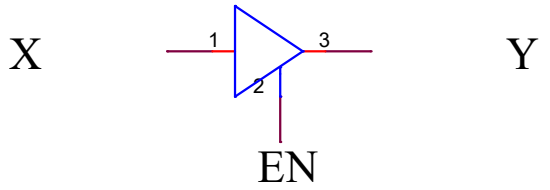
1 OF 3 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

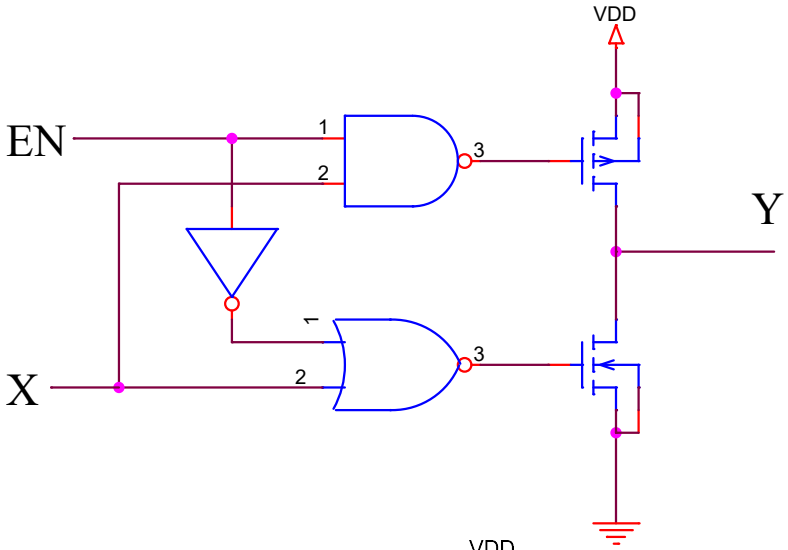


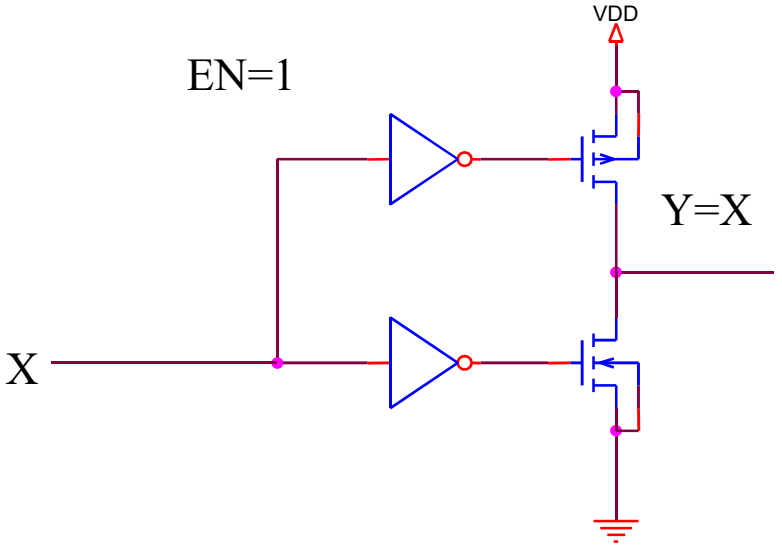
LOGIC DIAGRAM

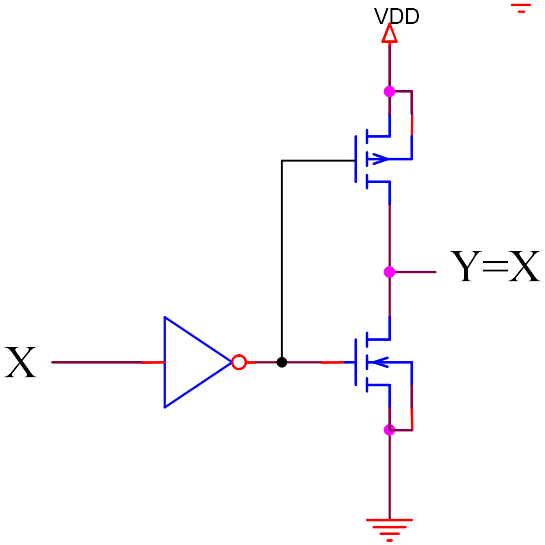
CD4025BMS

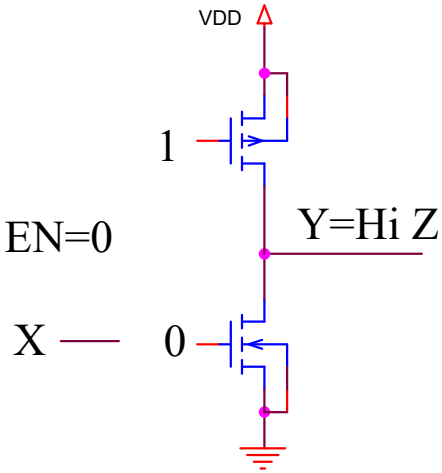
Trostatička kola



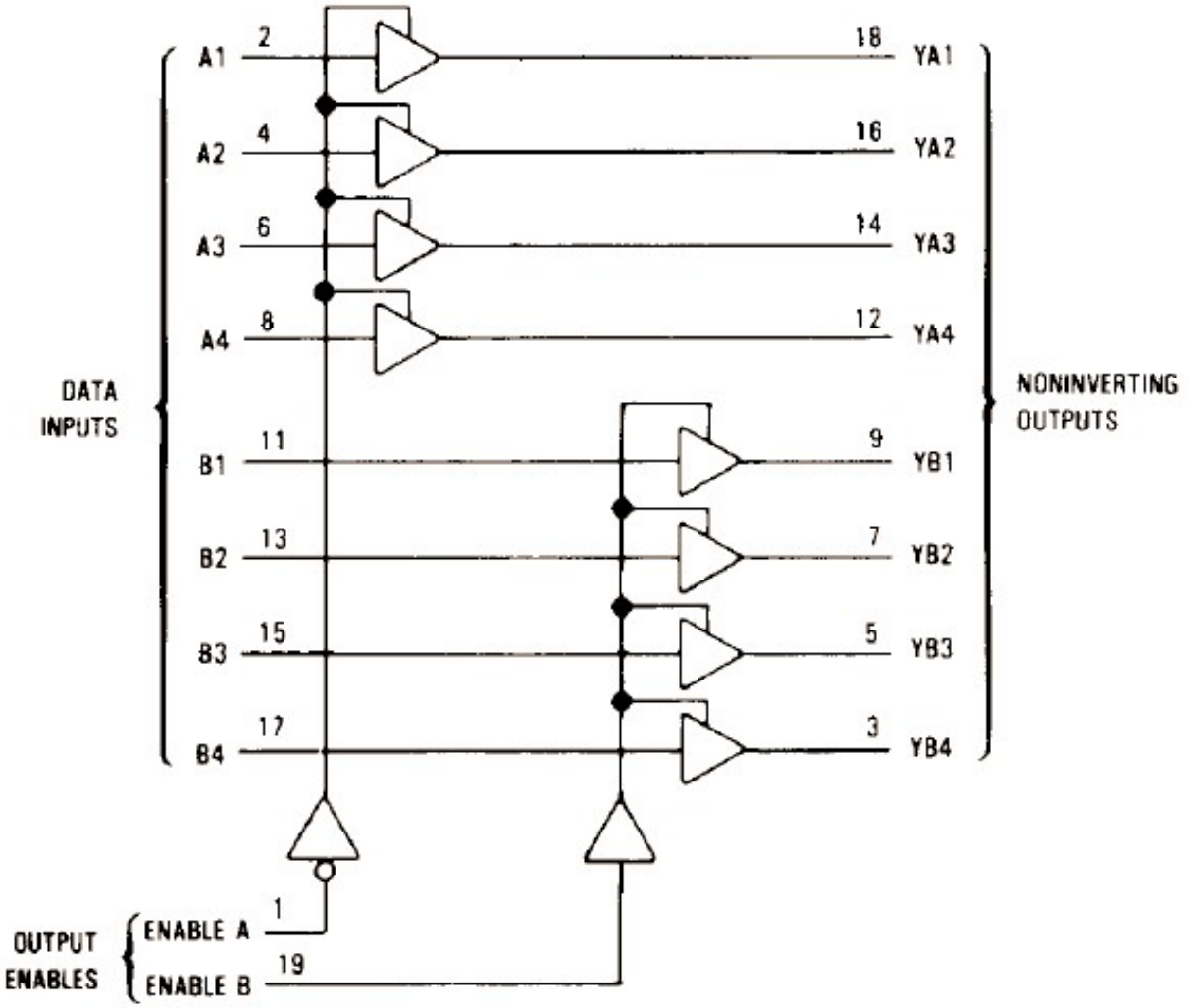




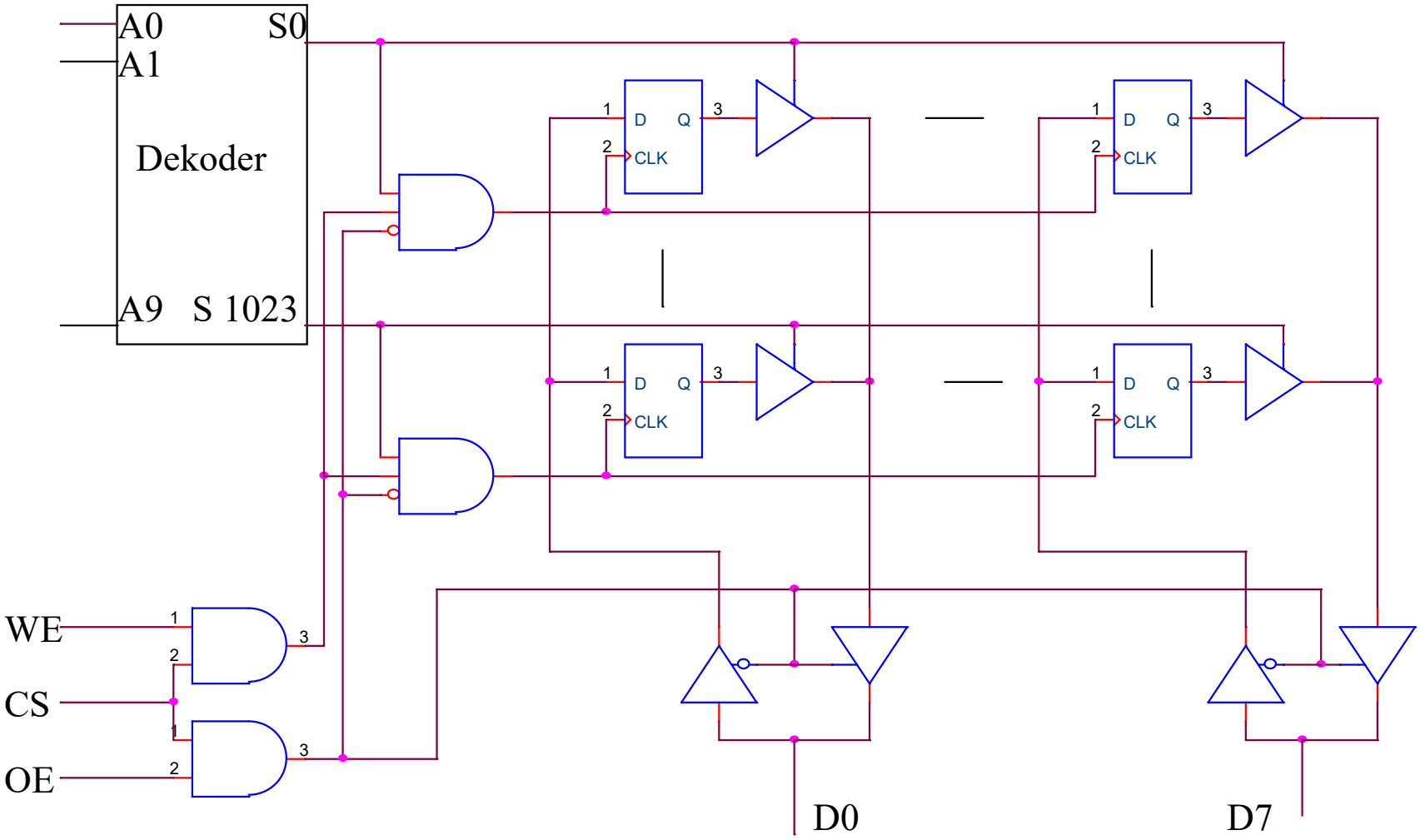




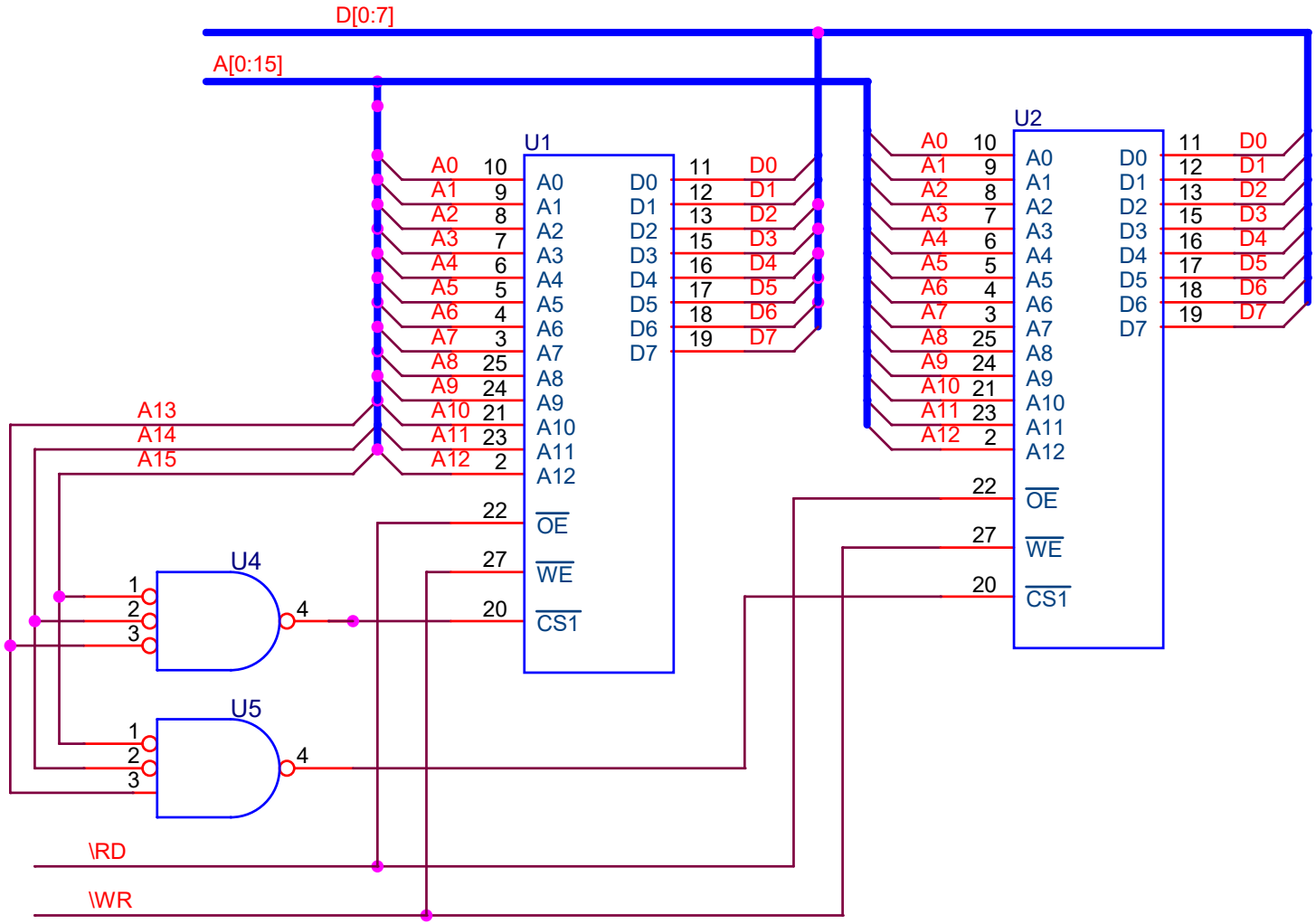
Integrisano kolo 74HC241



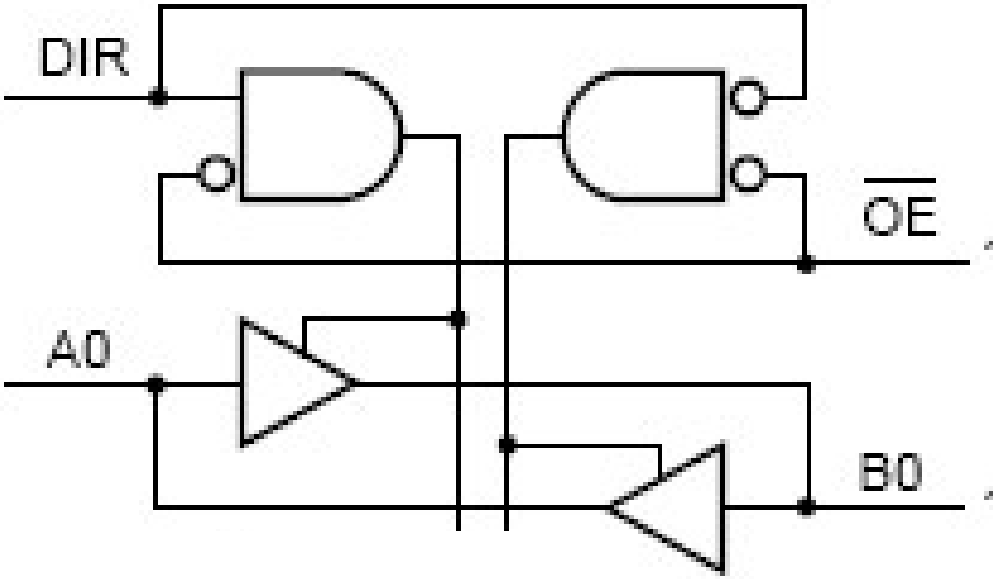
SRAM

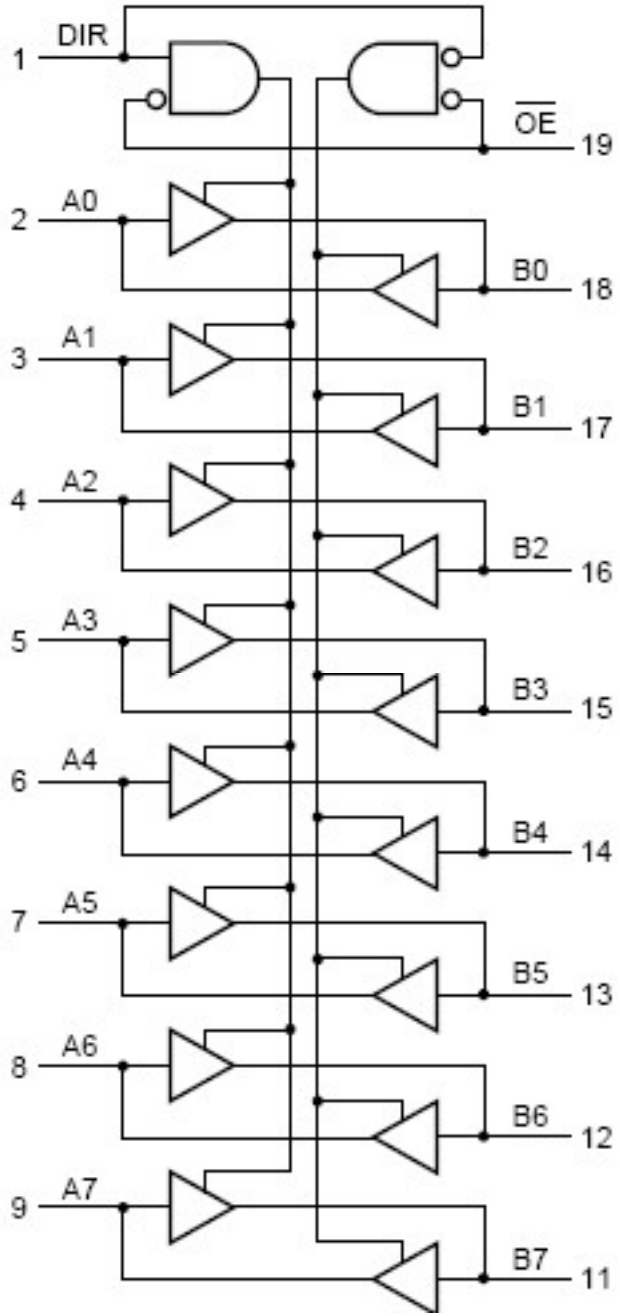


Povezivanje memorija na magistralu

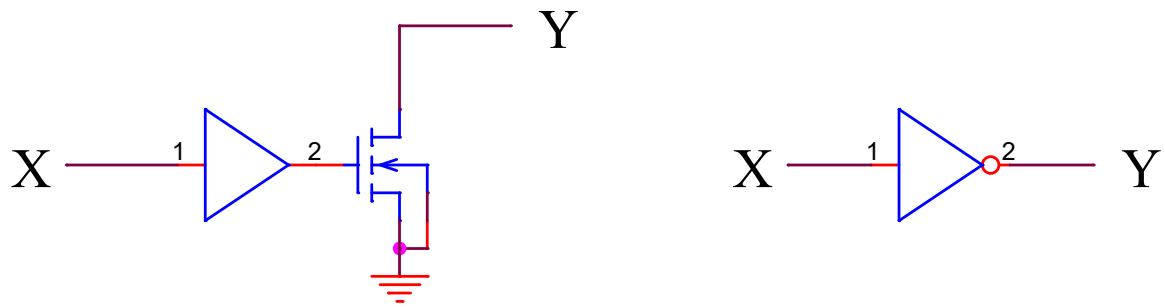


Bidirekcioni bafer 74HC245





Kola sa otvorenom drejnom (kolektorom)

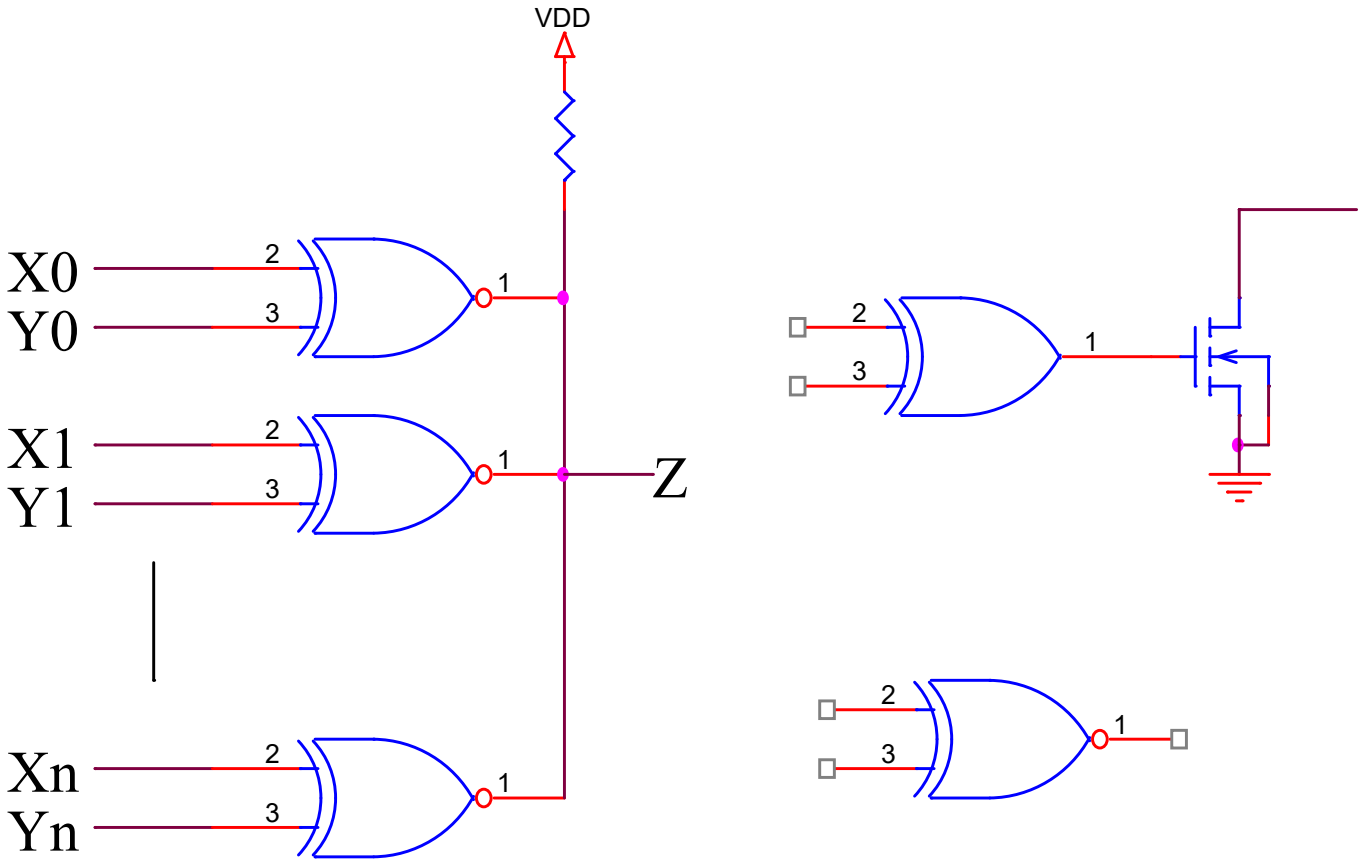


$$X = 1 \Rightarrow Y = 0$$

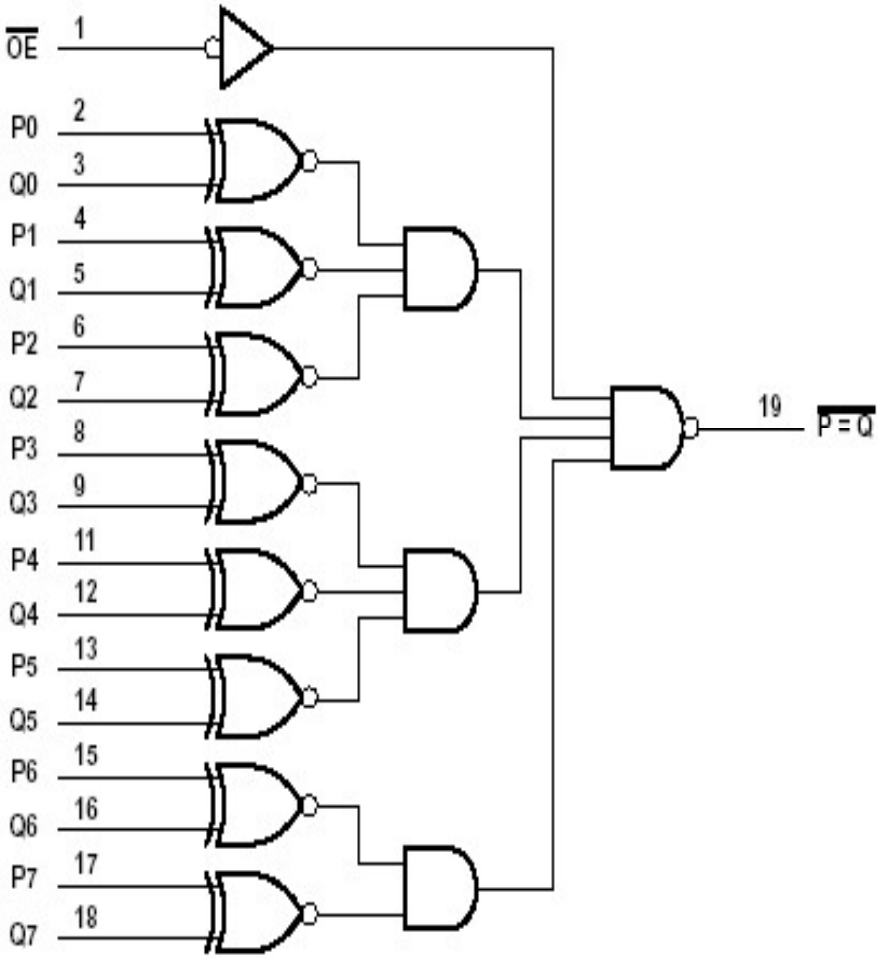
$$X = 0 \Rightarrow Y = \text{Hi Z}$$

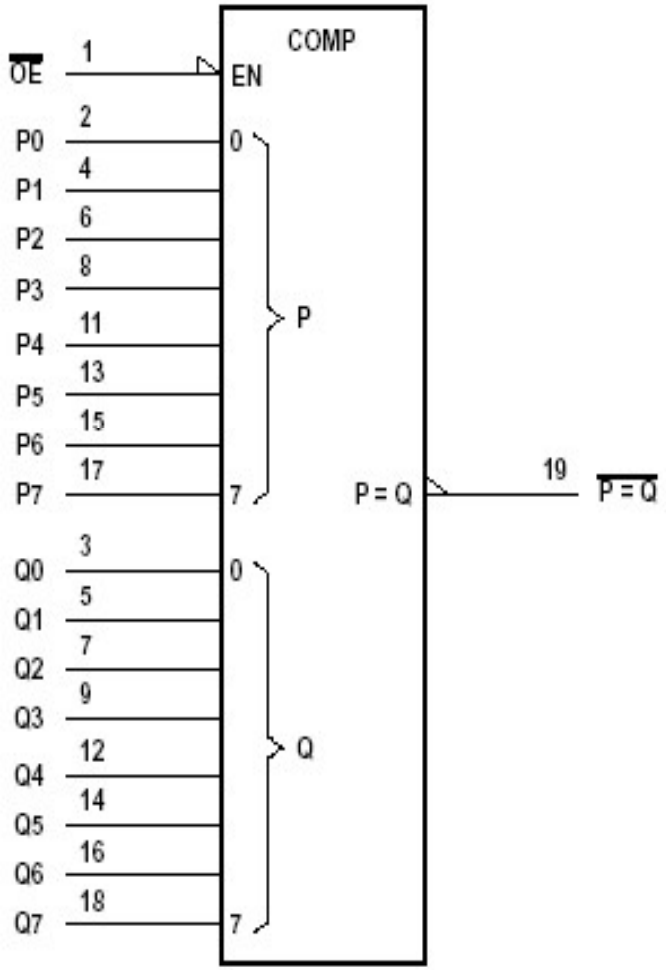
Kod TTL logike, na izlazu je NPN tranzistor

Primena – wired OR logika
Primer 1: komparator



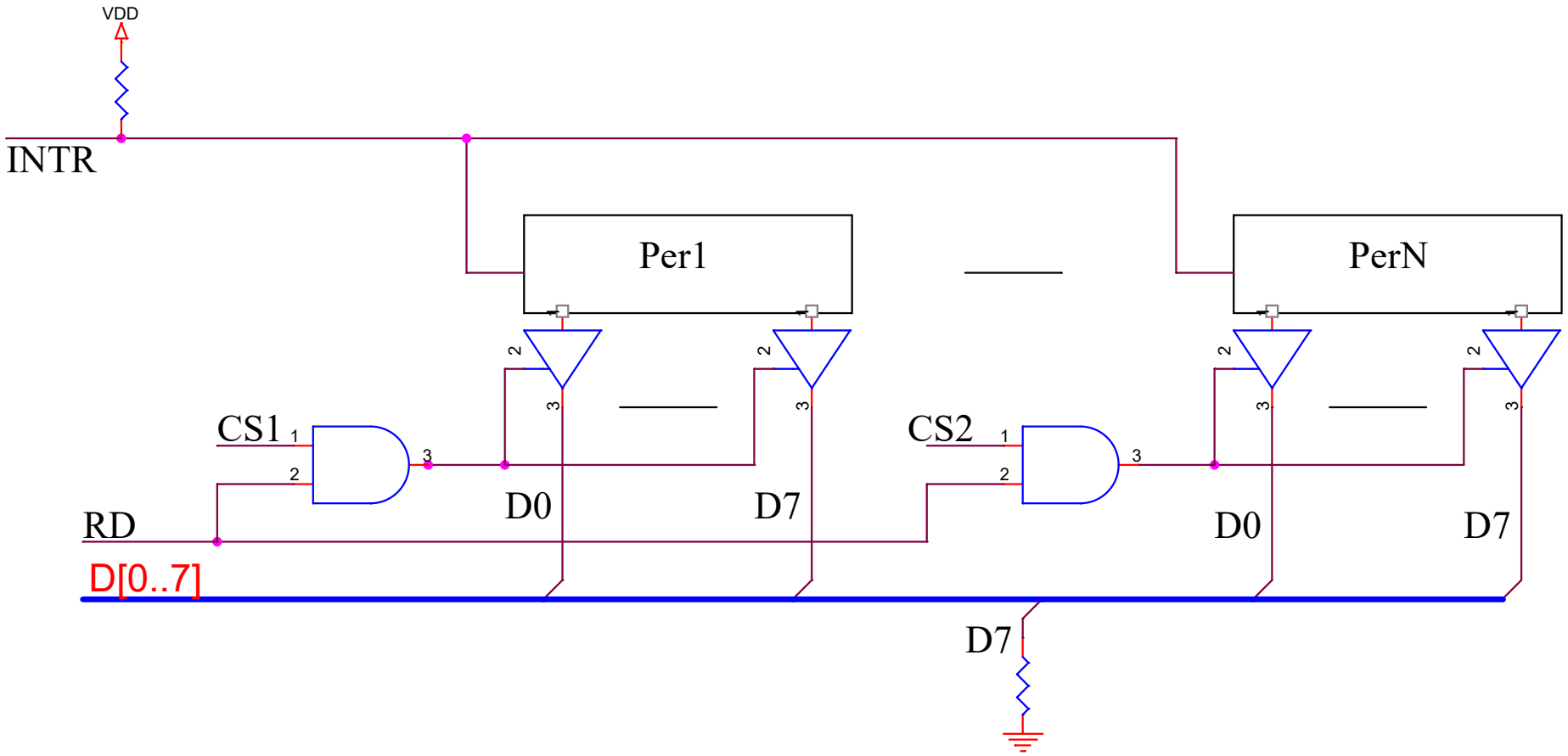
Alternativna klasična realizacija



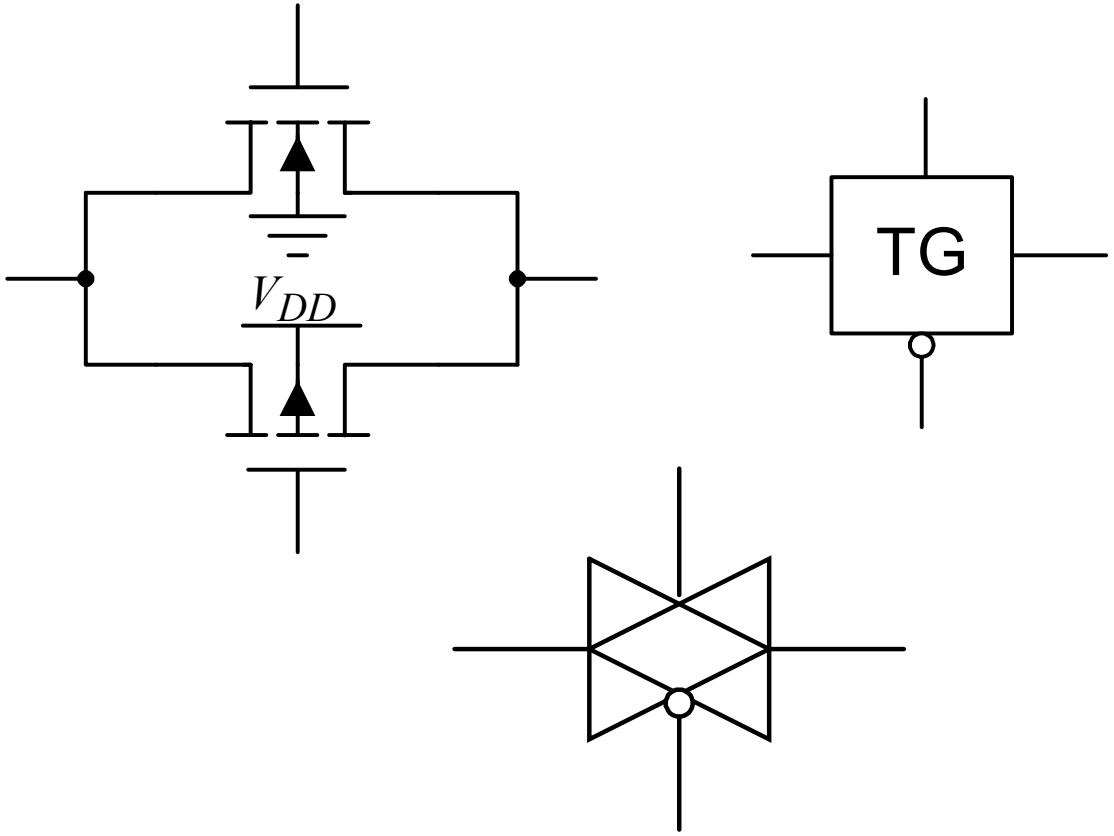


Primer 2

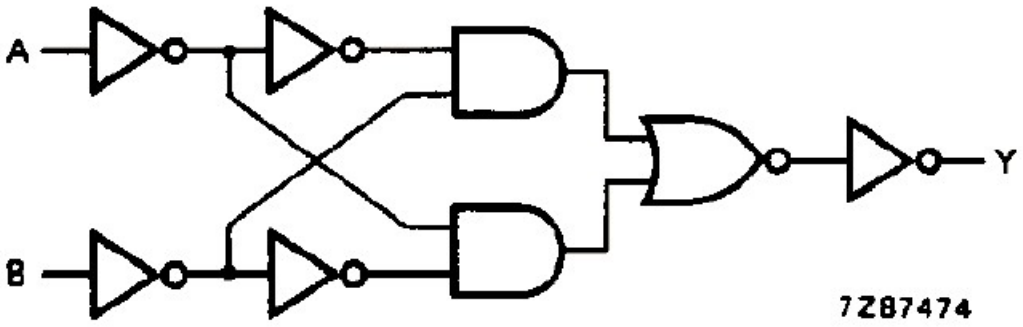
Zajednički prekid od više periferija (prekid je aktivan na log. nulu



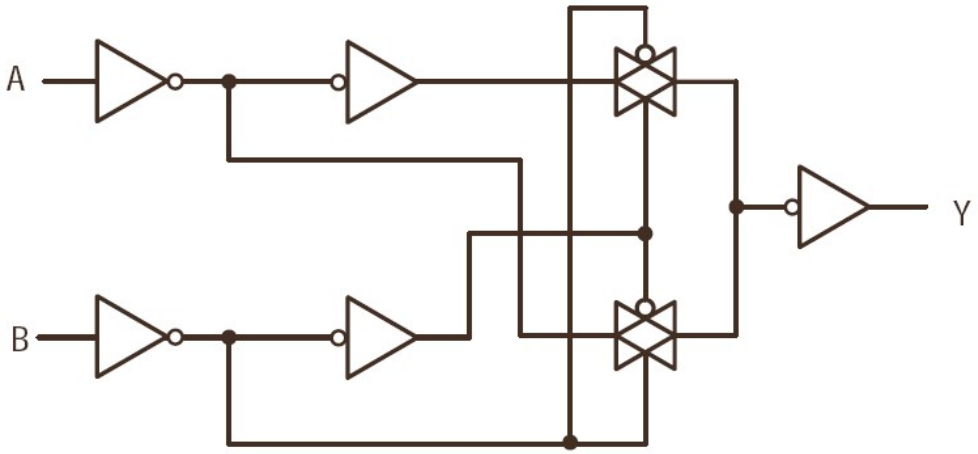
Bilateralni prekidač (transmisioni gejt)



Bilateralni prekidač i serijska logika: primer exor



XOR 74HC86

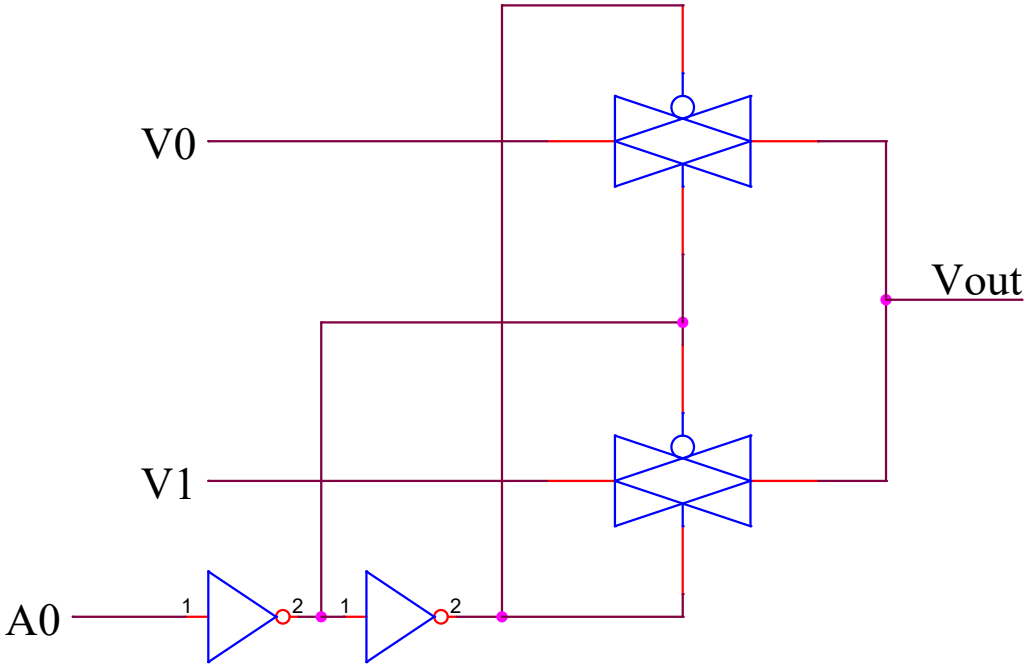


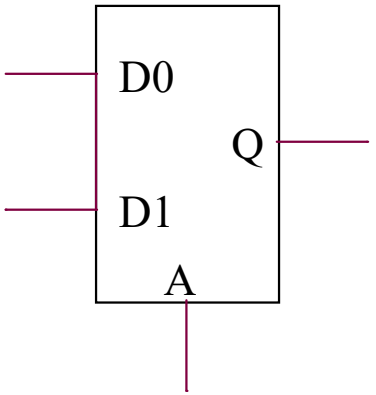
$$B = 1, Y = \overline{A}$$

$$B = 0, Y = A$$

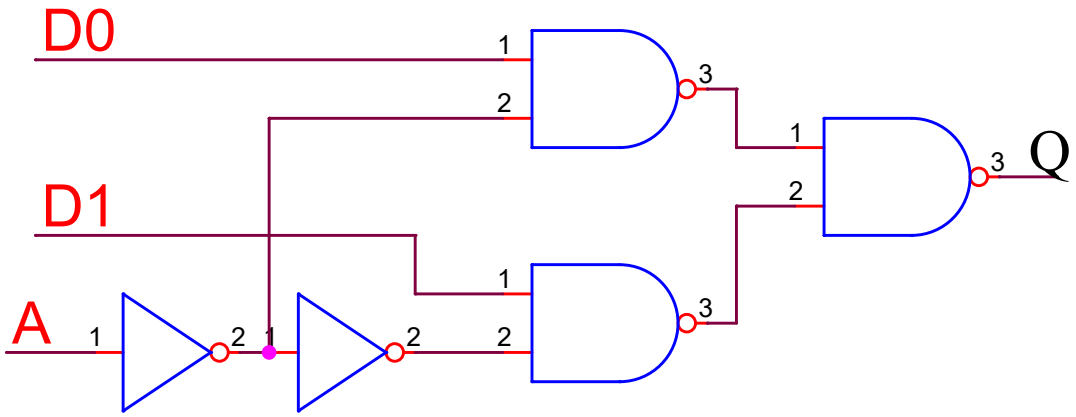
Ušteda u površini, potrošnji

Analogni multiplekser-demultiplekser 2/1



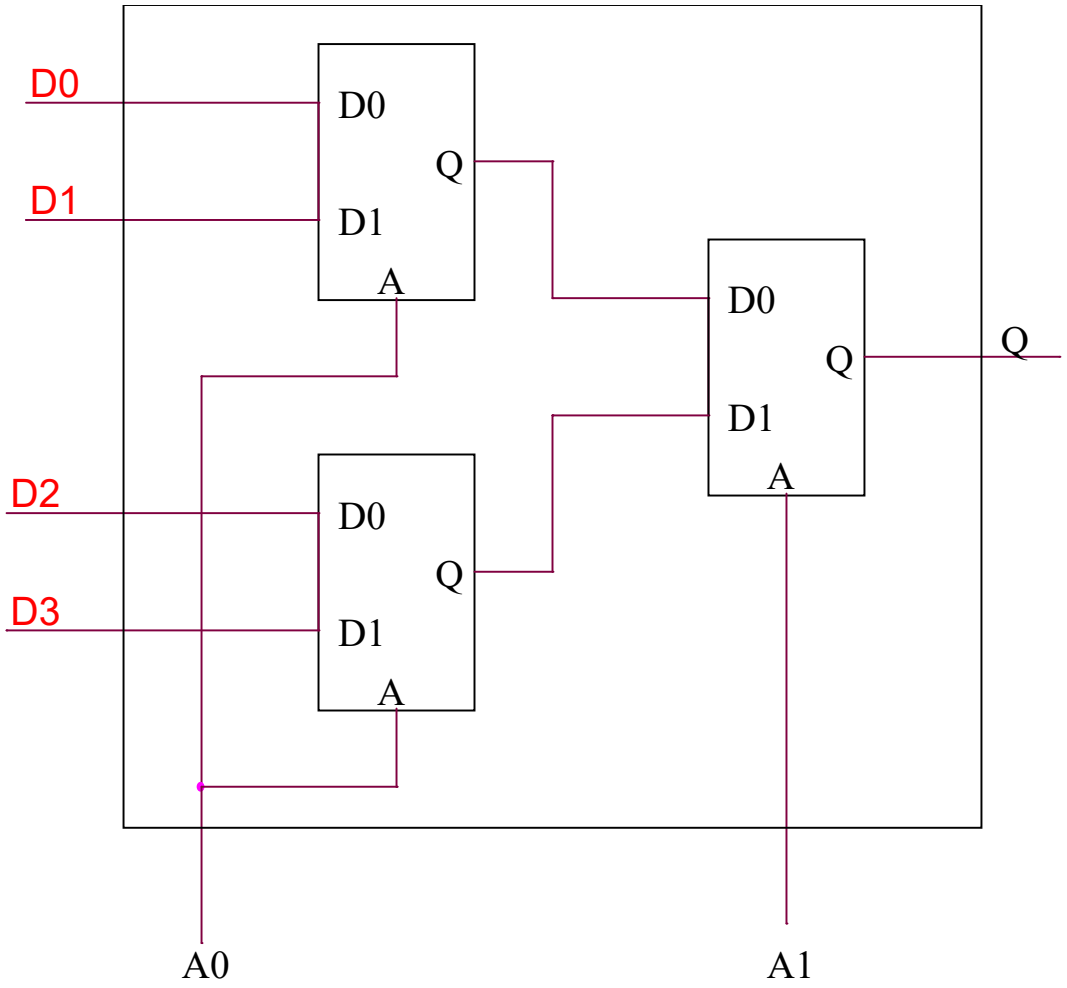


$$n_{tran} = 2 \times 2\big|_{prekidaci} + 2 \times 2_{invertori} = 8$$



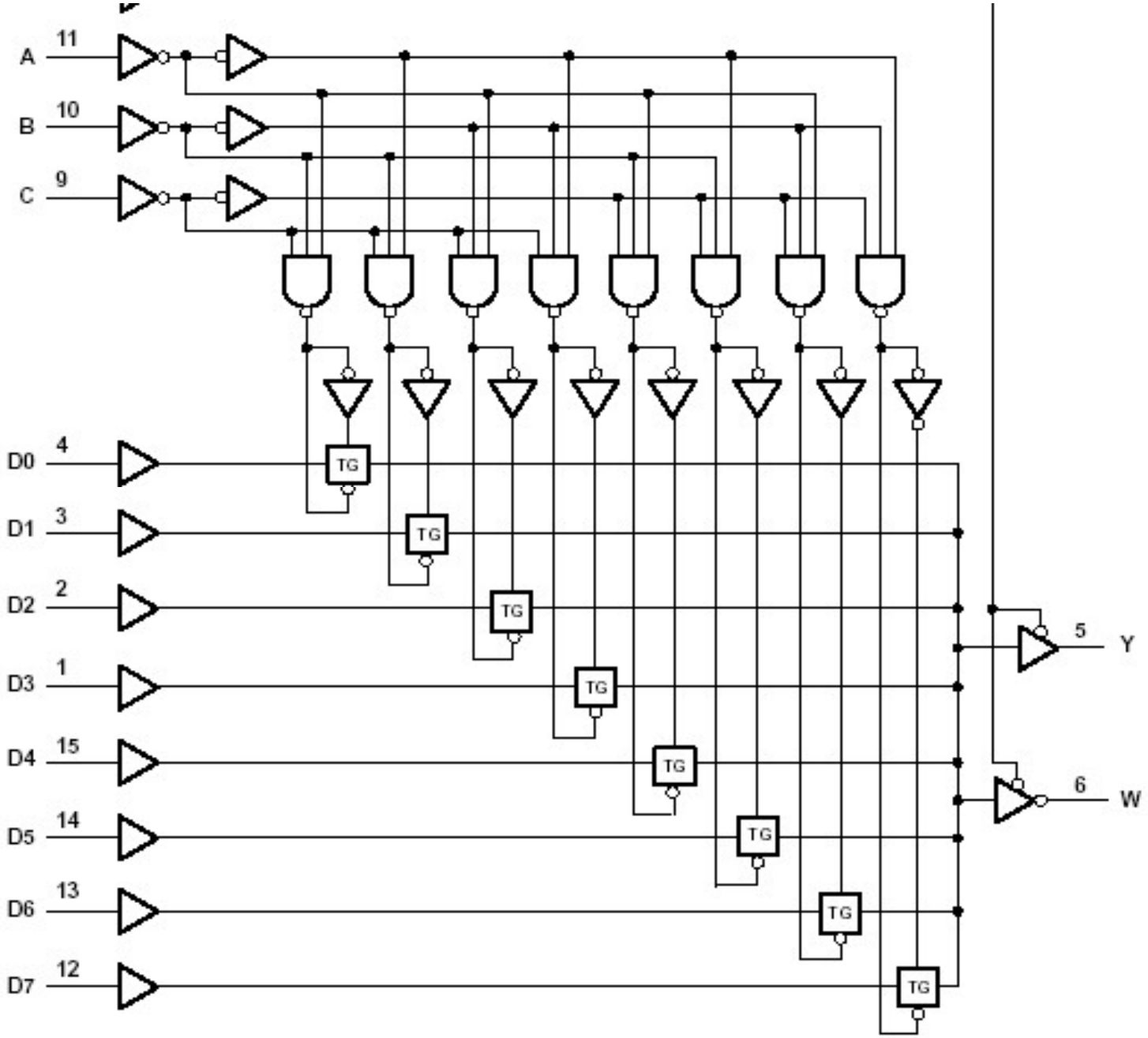
$$n_{tran} = 3 \times 4\big|_{NI} + 2 \times 2_{invertori} = 16$$

Mux 4/1

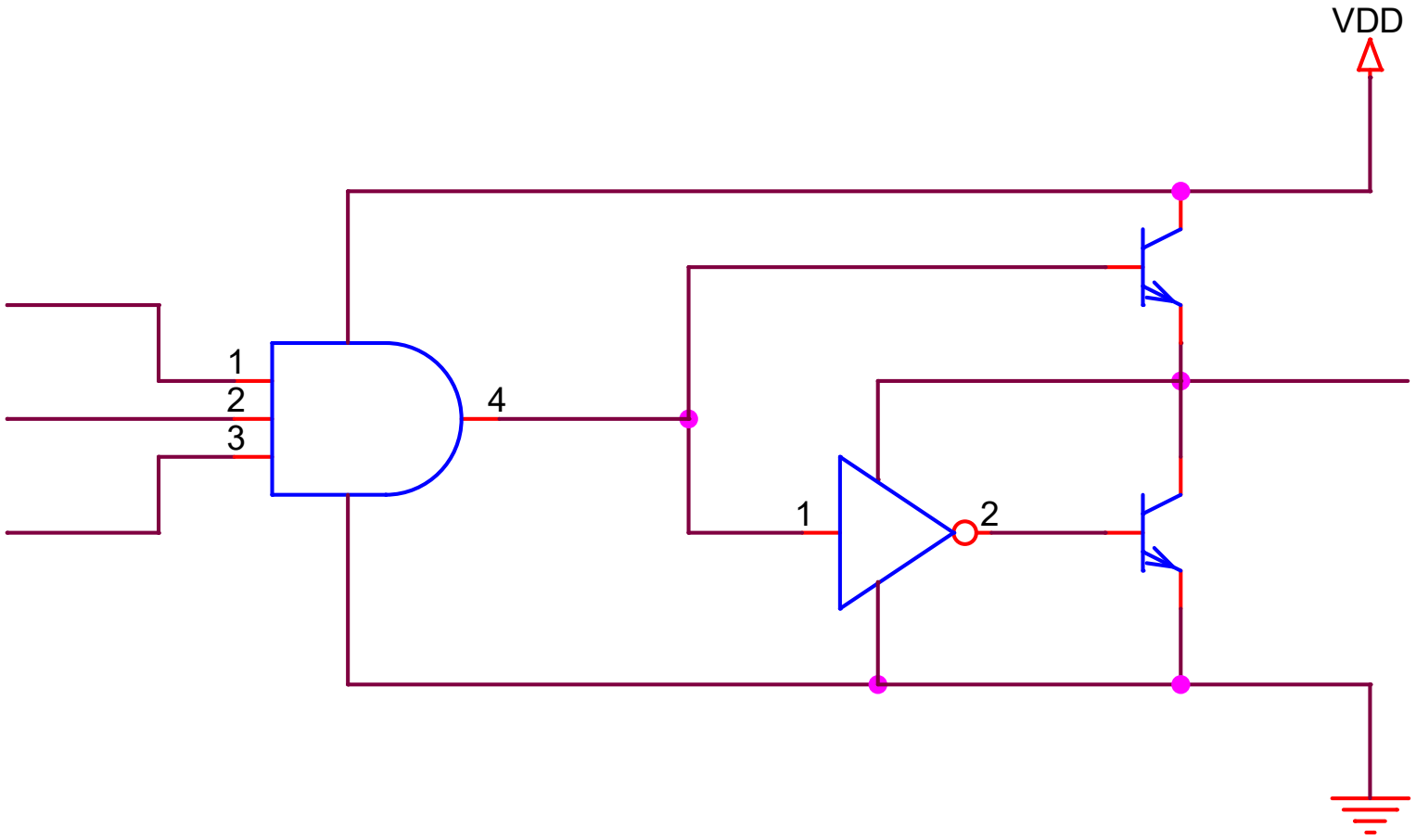


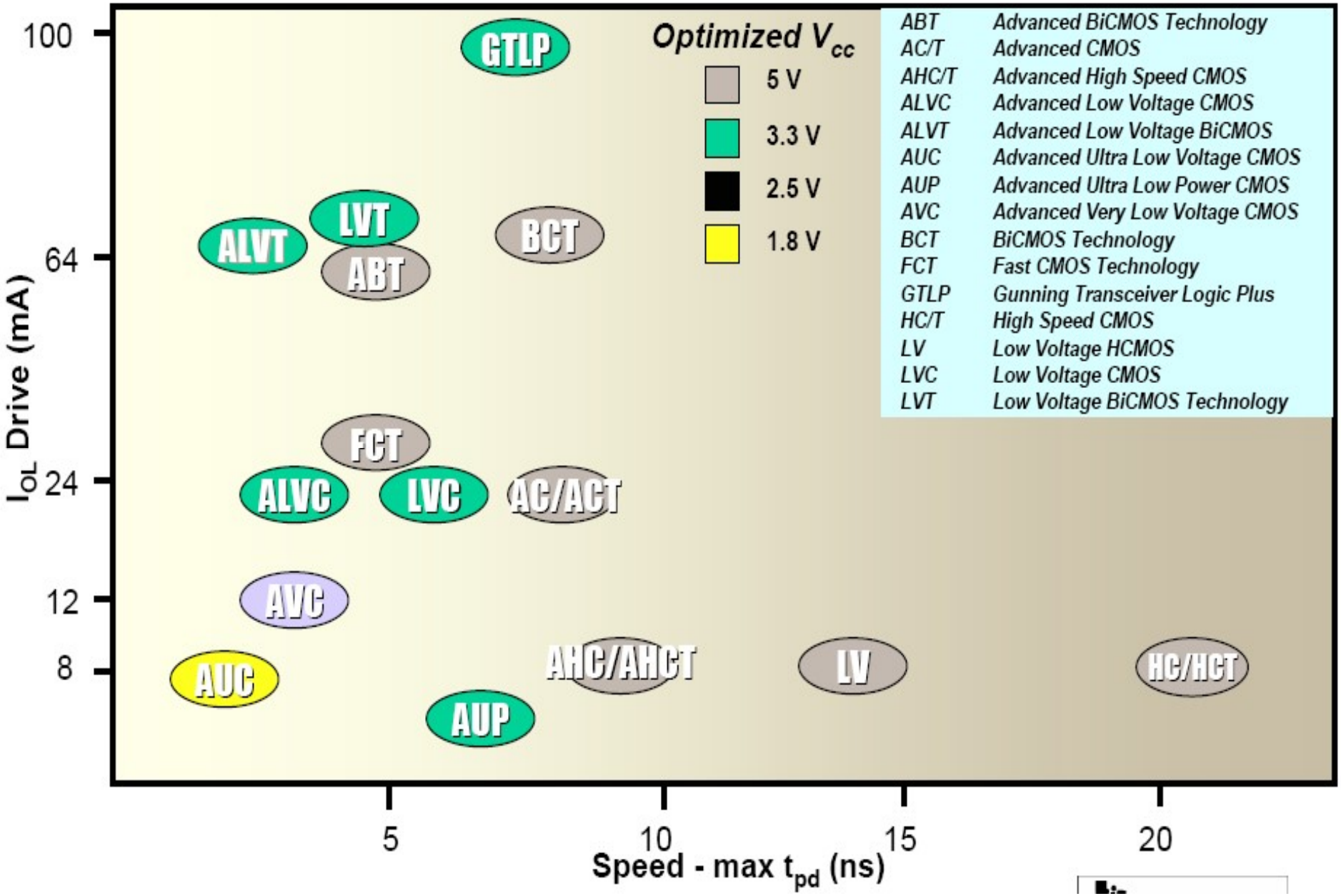
$$n_{tran} = 3 \times 4\big|_{prekidaci} + 2 \times 4\big|_{invertori} = 20$$

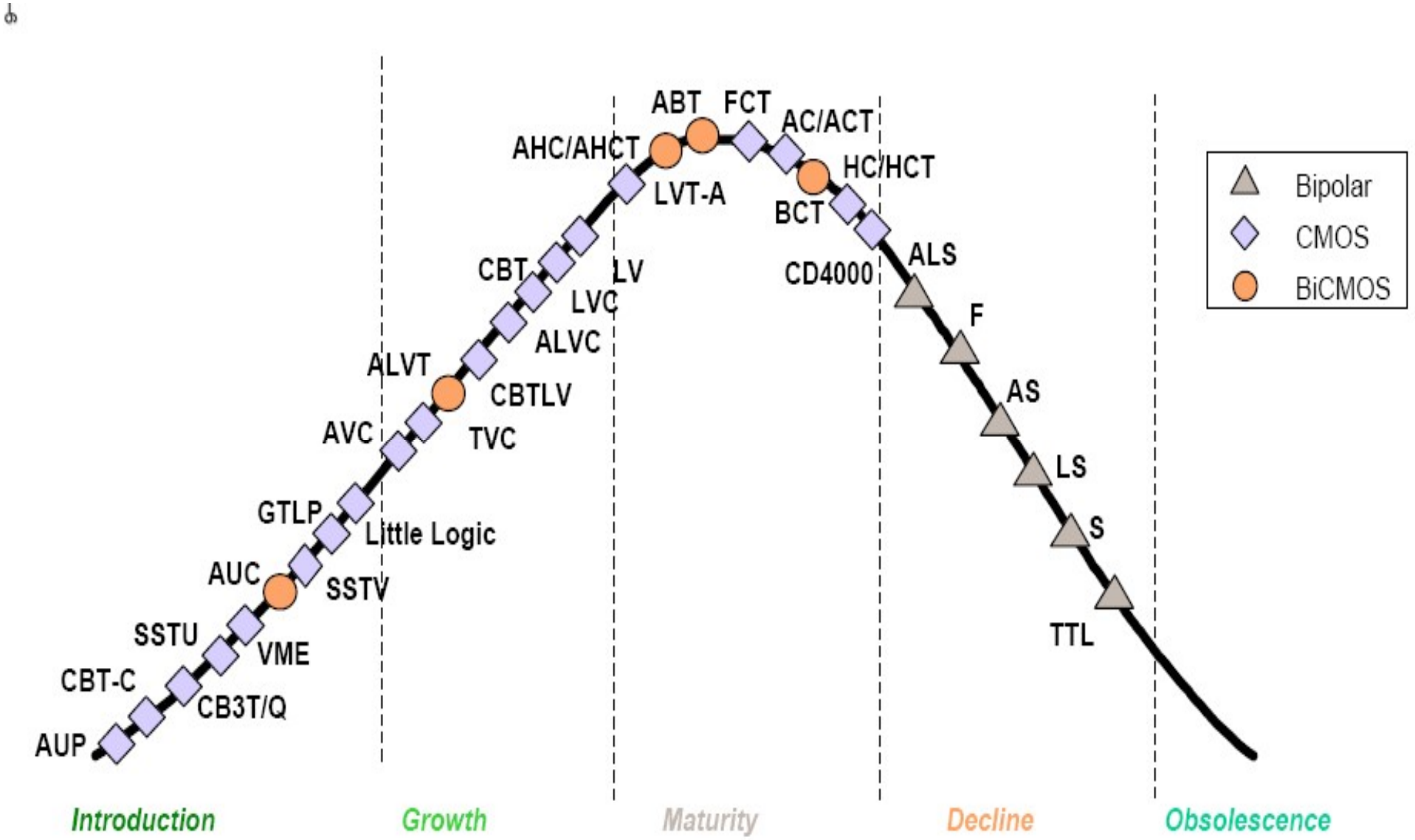
$$n_{tran}* = 3 \times 12\big|_{NI} + 2 \times 4\big|_{invertori} = 44$$


A
11
B
10
C
9
D0
4
D1
3
D2
2
D3
1
D4
15
D5
14
D6
13
D7
12
TG
5
Y
6
W

BICMOS




100
64
24
12
8
I_{OL} Drive (mA)
GTLP
ALVT
LVT
ABT
BCT
FCT
ALVC
LVC
AC/ACT
AVC
AUC
AUP
AHC/AHCT
LV
HC/HCT
Optimized V_{cc}
5 V
3.3 V
2.5 V
1.8 V
ABT Advanced BiCMOS Technology
AC/T Advanced CMOS
AHC/T Advanced High Speed CMOS
ALVC Advanced Low Voltage CMOS
ALVT Advanced Low Voltage BiCMOS
AUC Advanced Ultra Low Voltage CMOS
AUP Advanced Ultra Low Power CMOS
AVC Advanced Very Low Voltage CMOS
BCT BiCMOS Technology
FCT Fast CMOS Technology
GTLP Gunning Transceiver Logic Plus
HC/T High Speed CMOS
LV Low Voltage HCMOS
LVC Low Voltage CMOS
LVT Low Voltage BiCMOS Technology
5
10
15
20
Speed - max t_{pd} (ns)

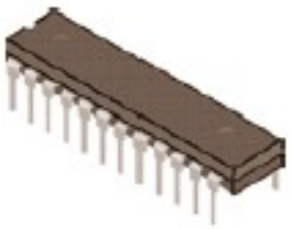

ABT
FCT
AC/ACT
AHC/AHCT
HC/HCT
LVT-A
BCT
CBT
LV
CD4000
ALS
LVC
ALVC
F
ALVT
CBTLV
AS
AVC
TVC
LS
GTLP
Little Logic
S
AUC
SSTV
TTL
SSTU
VME
CBT-C
CB3T/Q
AUP
Bipolar
CMOS
BiCMOS
Introduction
Growth
Maturity
Decline
Obsolescence

Family	Operating Voltage	Optimized Voltage	Prop $Delay_{typ}$	Output Drive	V_i Tolerant	I_{off}
AUC	0.8-2.7V	1.8V	2.0ns	8mA	3.6V	Yes
AUP	0.8-3.6V	3.3V	5.4ns	4mA	3.6V	Yes
LVC	1.65-5.5V	3.3V	3.5ns	24mA	5.5V	Yes
AHC	2.0-5.5V	5.0V	5.0ns	8mA	5.5V	No
CBT	4.5-5.5V	5.0V	0.25ns	n/a	5.5V	n/a
CBTD	4.5-5.5V	5.0V	0.25ns	n/a	5.5V	n/a
CBTLV	2.3-3.6V	3.3V	0.25ns	n/a	3.6V	Yes

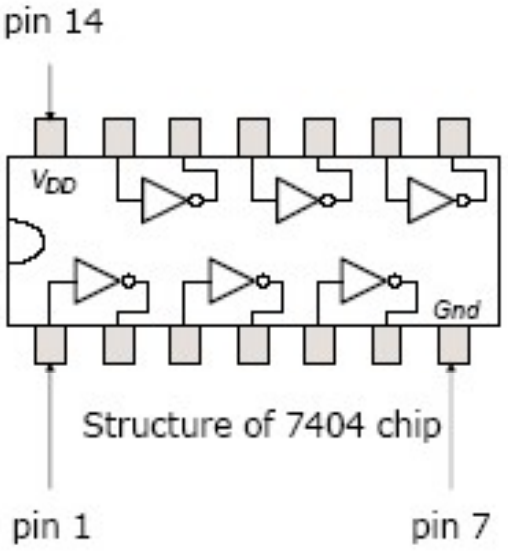
Ostale MOS tehnologije

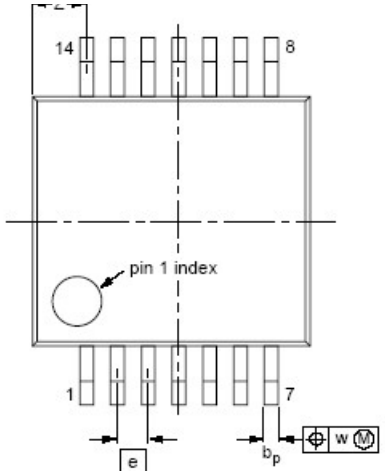
- NMOS / Pseudo NMOS
- SCL
- Dinamička logika
- Domino logika
- Adijabatska logika
- Clocked CMOS Logika (C 2 MOS).
- NP Domino Logika (Zipper CMOS).
- Cascade Voltage Switch Logika (CVSL).
- Source Follower Pull-up Logika (SFPL).

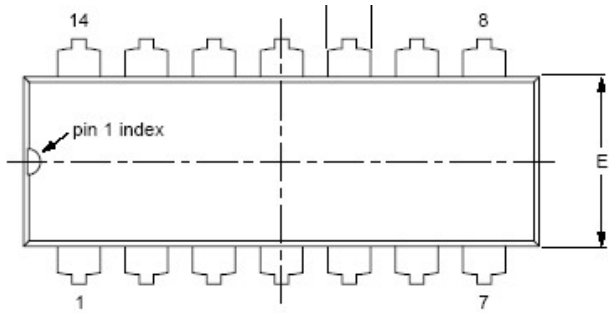
Kola niskog i srednjeg stepena integracije
Pakovanje



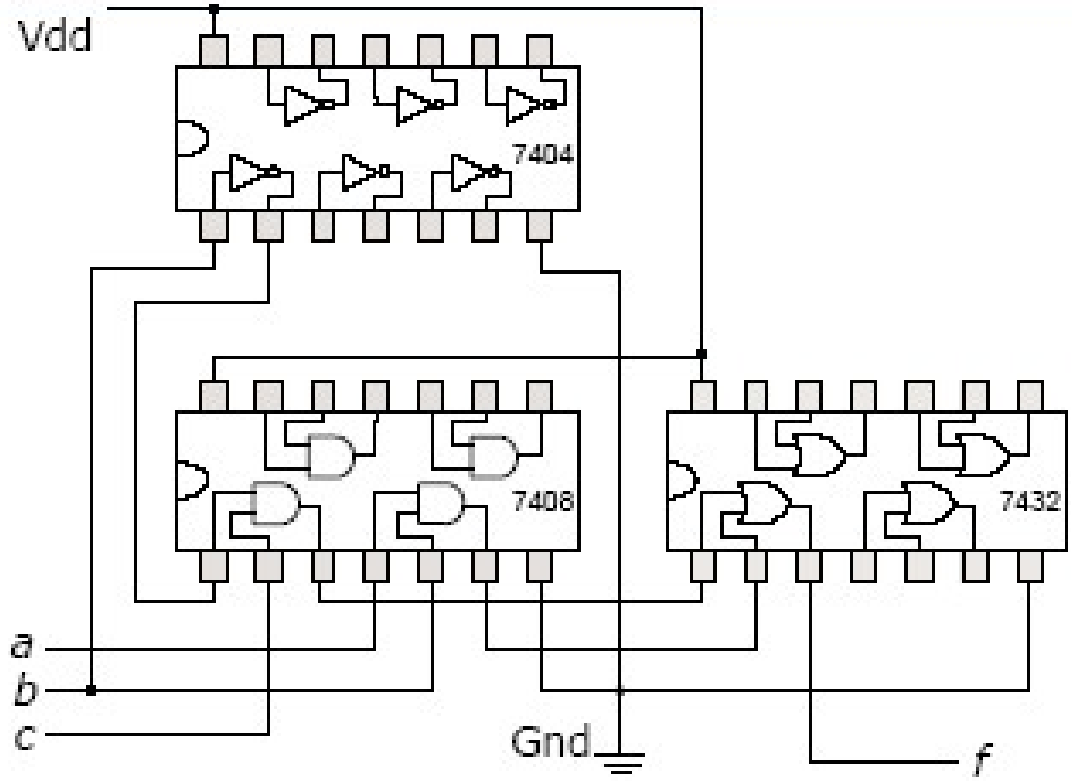
Dual-inline package







Implementation of f=ab+b'c



Ne isplati se ni po jednom kritetijumu = ne radi se!