
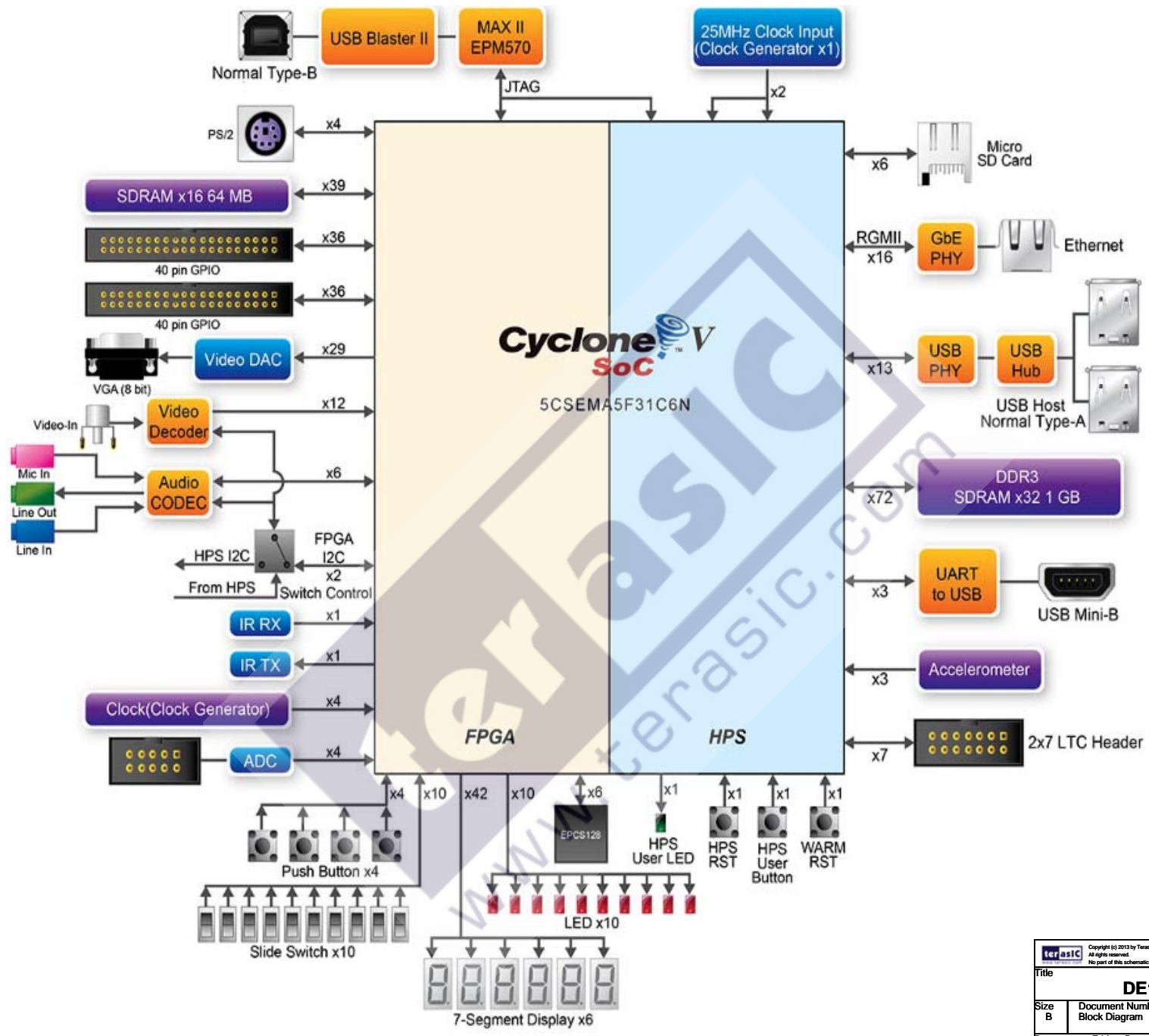


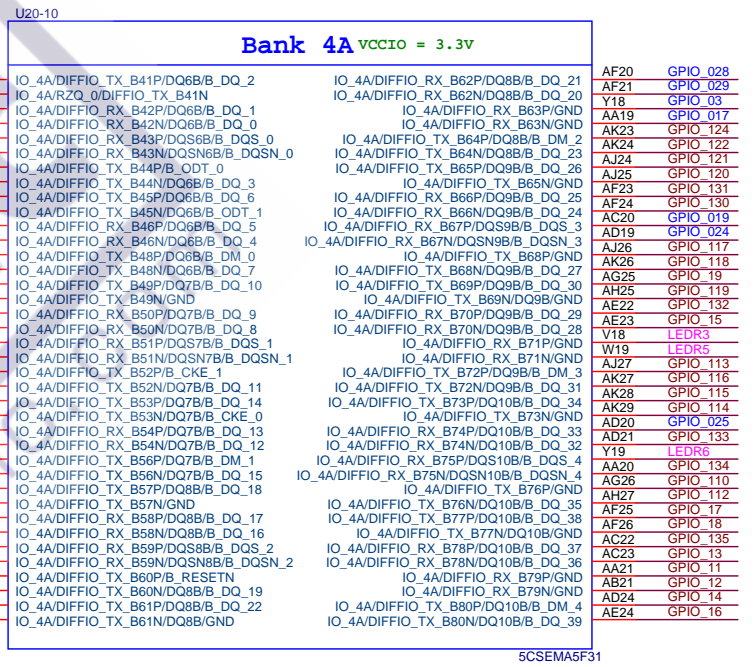
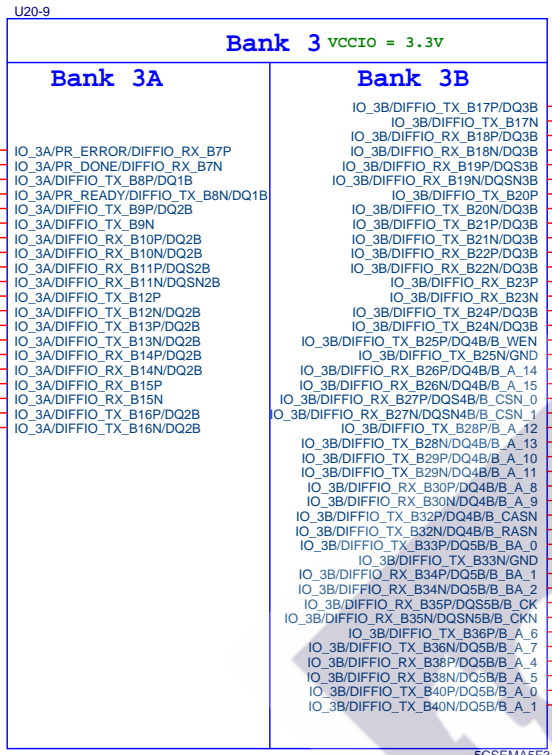
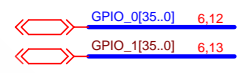
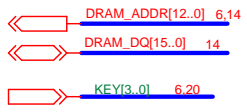
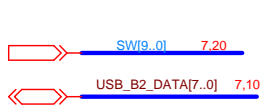
ALTERA Cyclone V SoC Development & Education Board (DE1-SoC)

PAGE	CONTENT	PAGE	CONTENT
1	Cover Page	16	ADV7123 VGA
2	Block Diagram	17	ADV7180 Video Decoder
3	FPGA BANK 3, BANK 4	18	Audio CODEC
4	FPGA BANK 5, BANK 6	19	7-Segment Display, LED
5	FPGA BANK 7, BANK 8	20	FPGA BUTTON, Switch
6	FPGA Clocks, GND	21	ADC, PS2, IR Tx, IR Rx
7	FPGA Configuration	22	2-port USB Host
8	FPGA Decoupling	23	1 Gigabit Ethernet
9	FPGA Power	24	UART to USB, SD CARD
10	USB Blaster II	25	Accelerometer, LTC Connector
11	JTAG Chain	26	I2C Multiplexer, HPS BUTTON, HPS LED
12	GPIO 0	27	Power - 1.1V
13	GPIO 1	28	Power - 5V, 3.3V
14	SDRAM, HPS QSPI Flash	29	Power - 9V, 2.5V, 1.5V
15	HPS DDR3 SDRAM	30	Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT

 <small>Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</small>		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Cover Page	E
Date:	Monday, October 20, 2014	Sheet 1 of 30



Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Block Diagram	E
Date:	Friday, December 19, 2014	Sheet 2 of 30

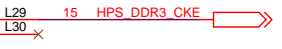
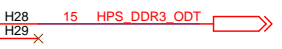
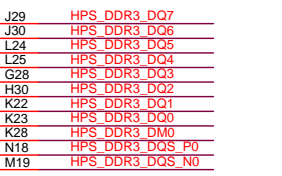
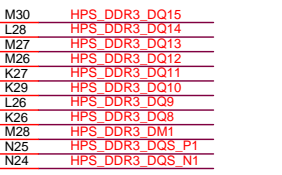
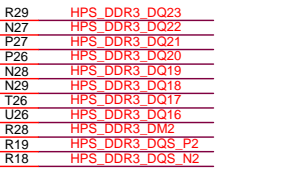
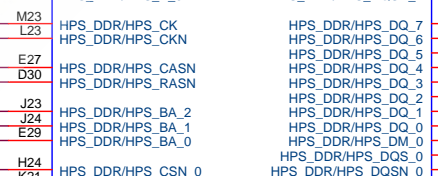
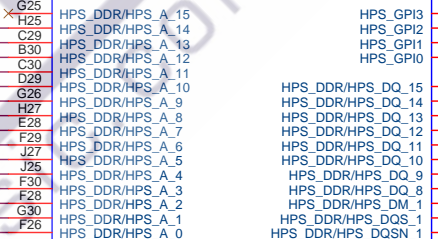
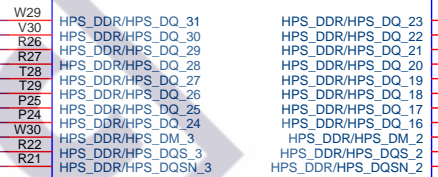
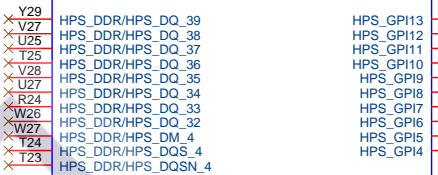
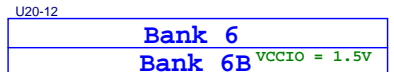
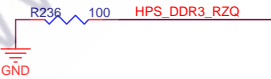
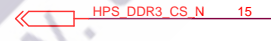
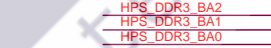
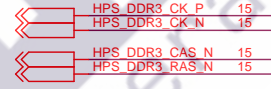
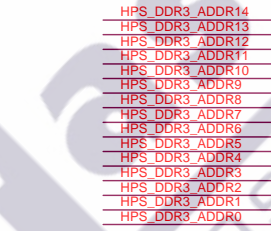
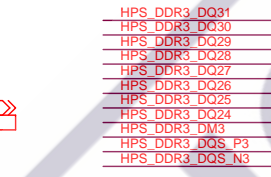
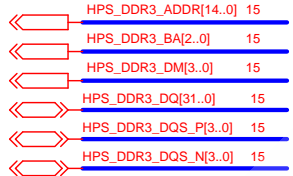
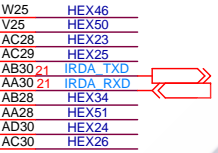
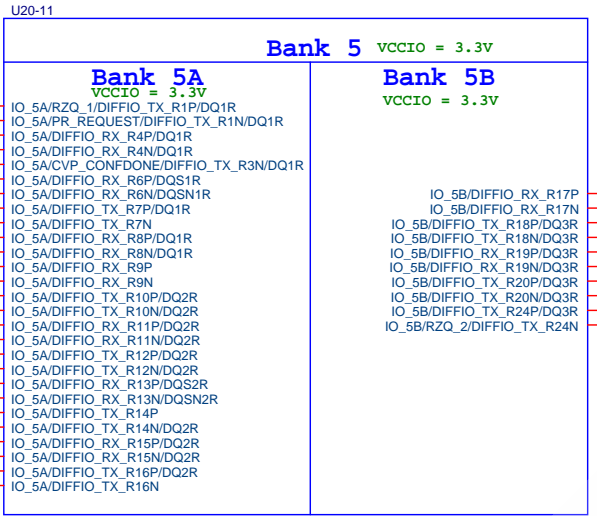
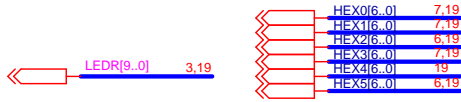


terasic Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DE1-SoC Board**

Size B Document Number: **FPGA BANK 3, BANK 4** Rev E

Date: **Monday, October 20, 2014** Sheet **3** of **30**



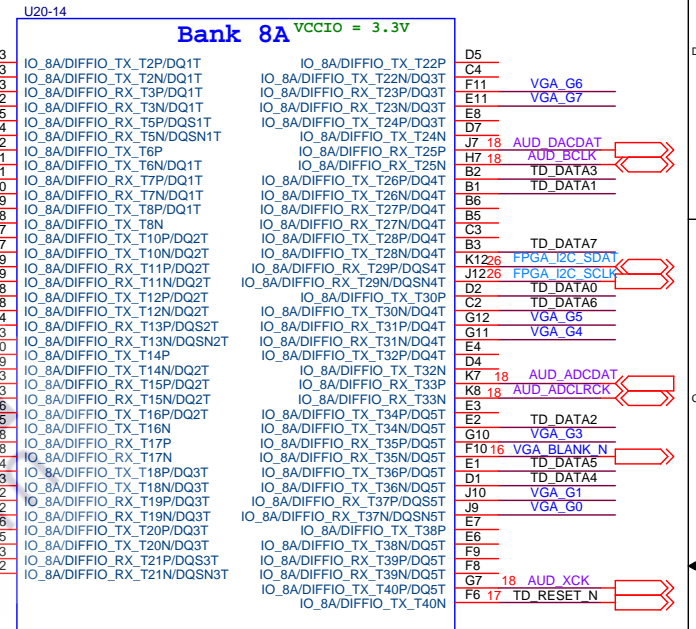
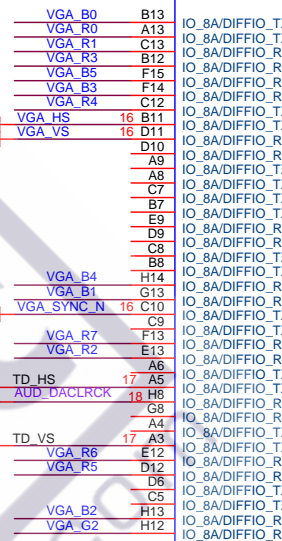
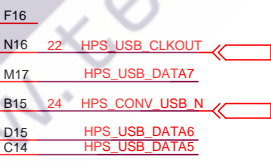
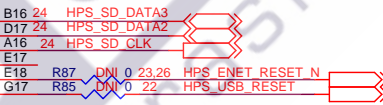
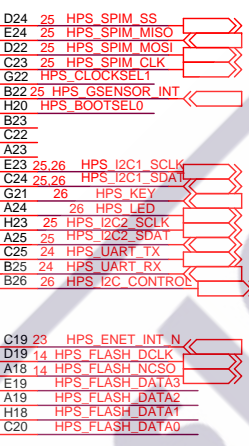
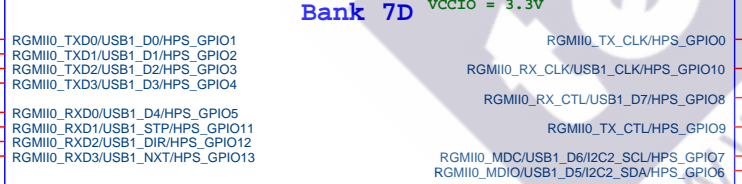
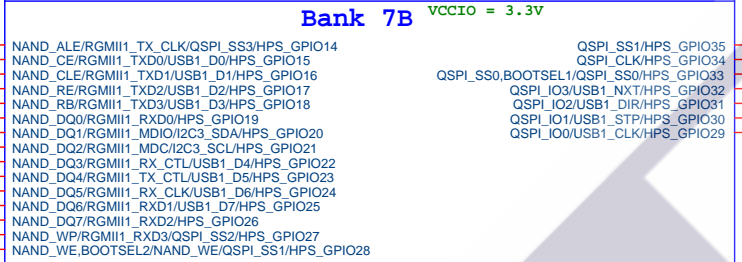
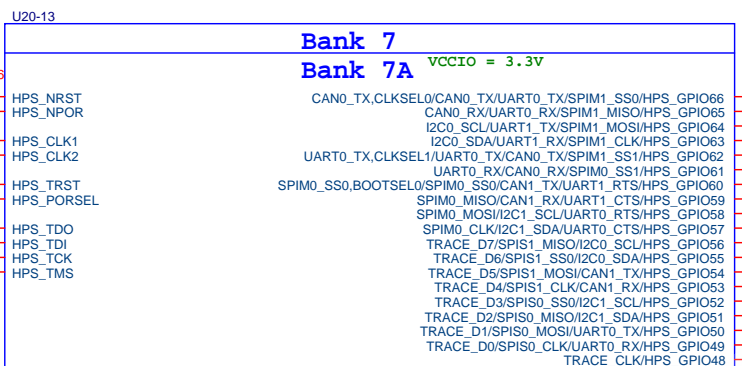
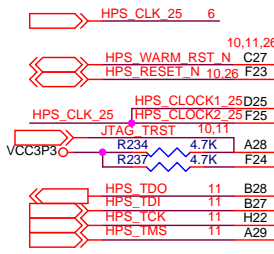
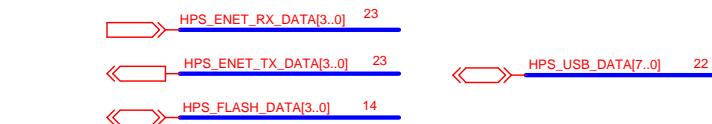
5CSEMA5F31

terasic Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

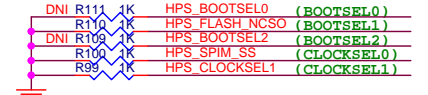
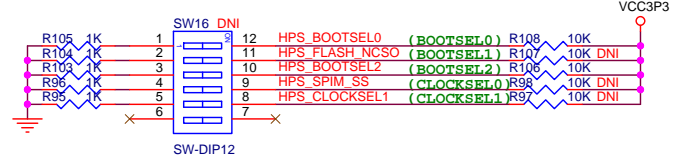
Title: **DE1-SoC Board**

Size B Document Number: **FPGA BANK 5, BANK 6** Rev E

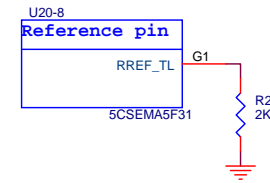
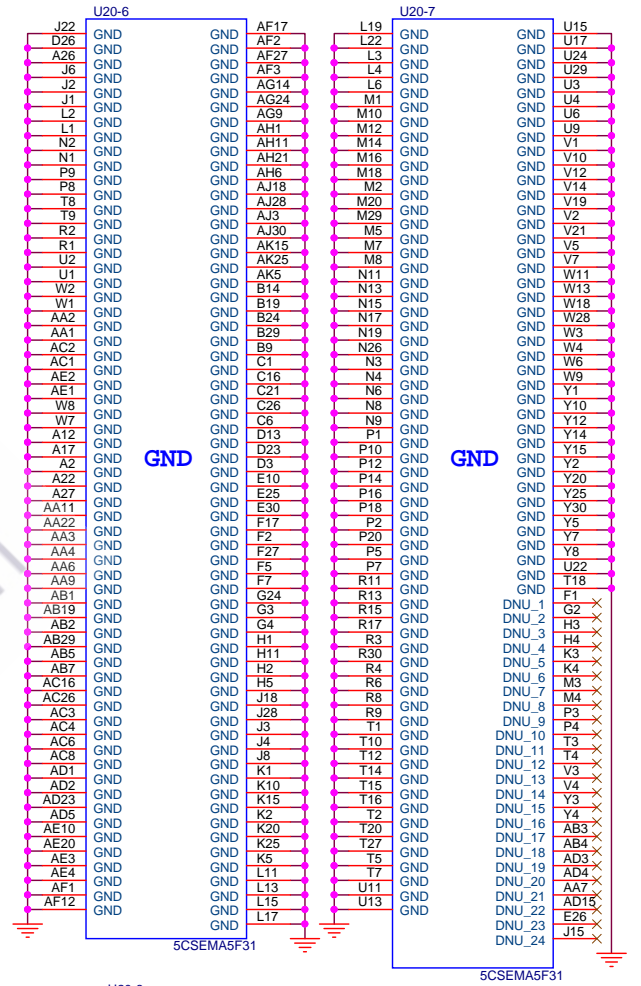
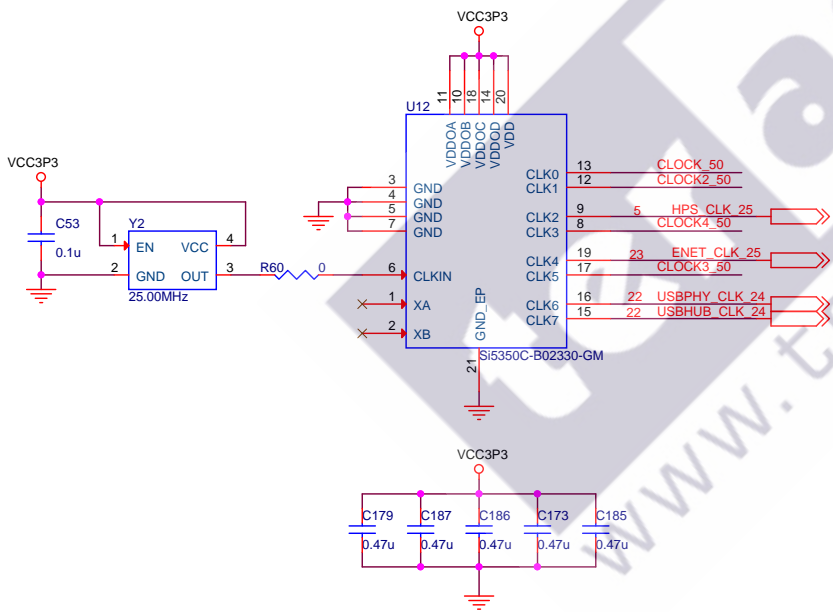
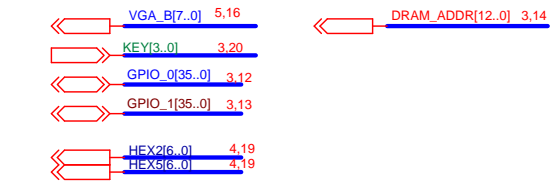
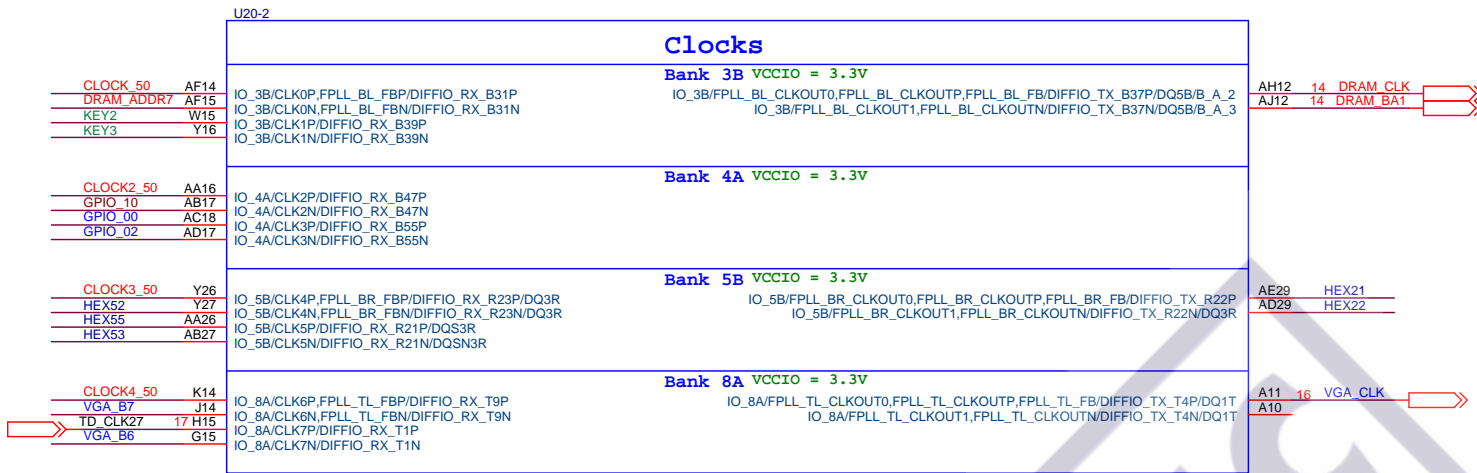
Date: **Monday, October 20, 2014** Sheet 4 of 30



Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
 CLKSEL[1:0]=0



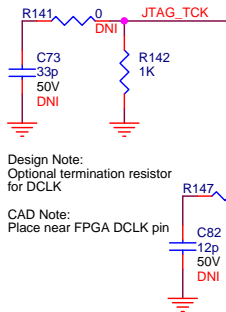
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
DE1-SoC Board		
Size B	Document Number FPGA BANK 7, BANK 8	Rev E
Date:	Monday, October 20, 2014	Sheet 5 of 30



terasic			Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title					
DE1-SoC Board					
Size	Document Number				Rev
B	FPGA Clocks & GND				E
Date:	Monday, October 20, 2014			Sheet	6 of 30

USB Blaster

- FPGA TDI 11
- JTAG TMS 11
- JTAG TCK 11
- FPGA TDO 11

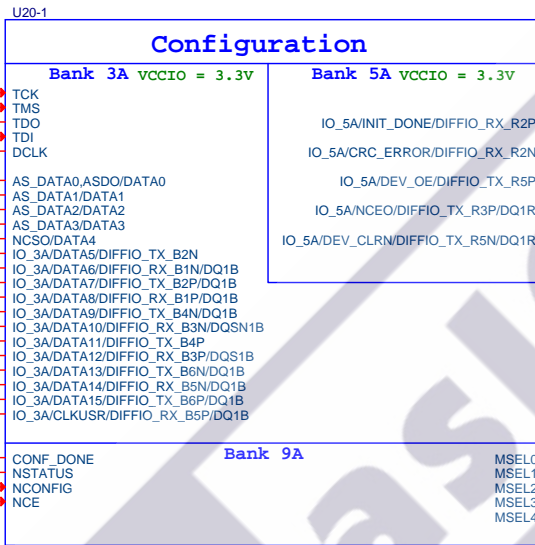


Design Note:
Optional termination resistor for DCLK

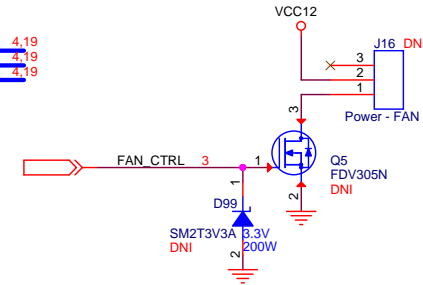
CAD Note:
Place near FPGA DCLK pin

- FPGA NCONFIG 10
- FPGA_CONF_DONE 10

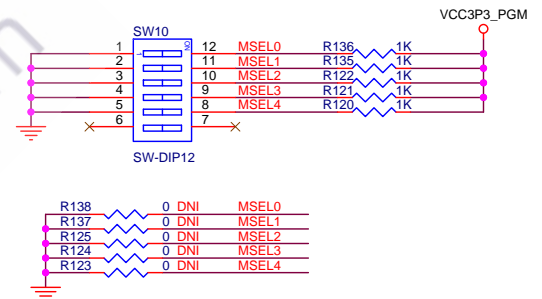
- USB_B2_DATA[7..0] 3,10
- SW[9..0] 3,20



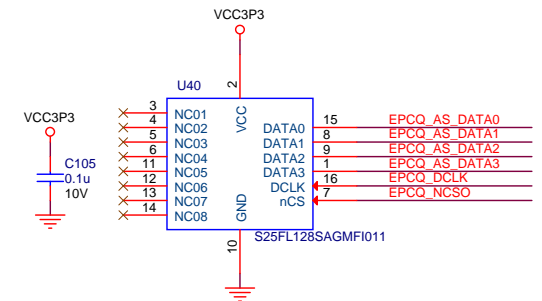
- HEX0[6..0] 4,19
- HEX1[6..0] 4,19
- HEX3[6..0] 4,19



Fix MSEL[4:0]=10010 in AS Fast Mode

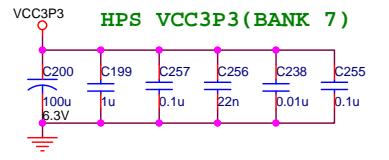
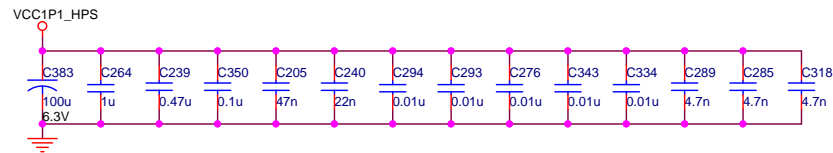
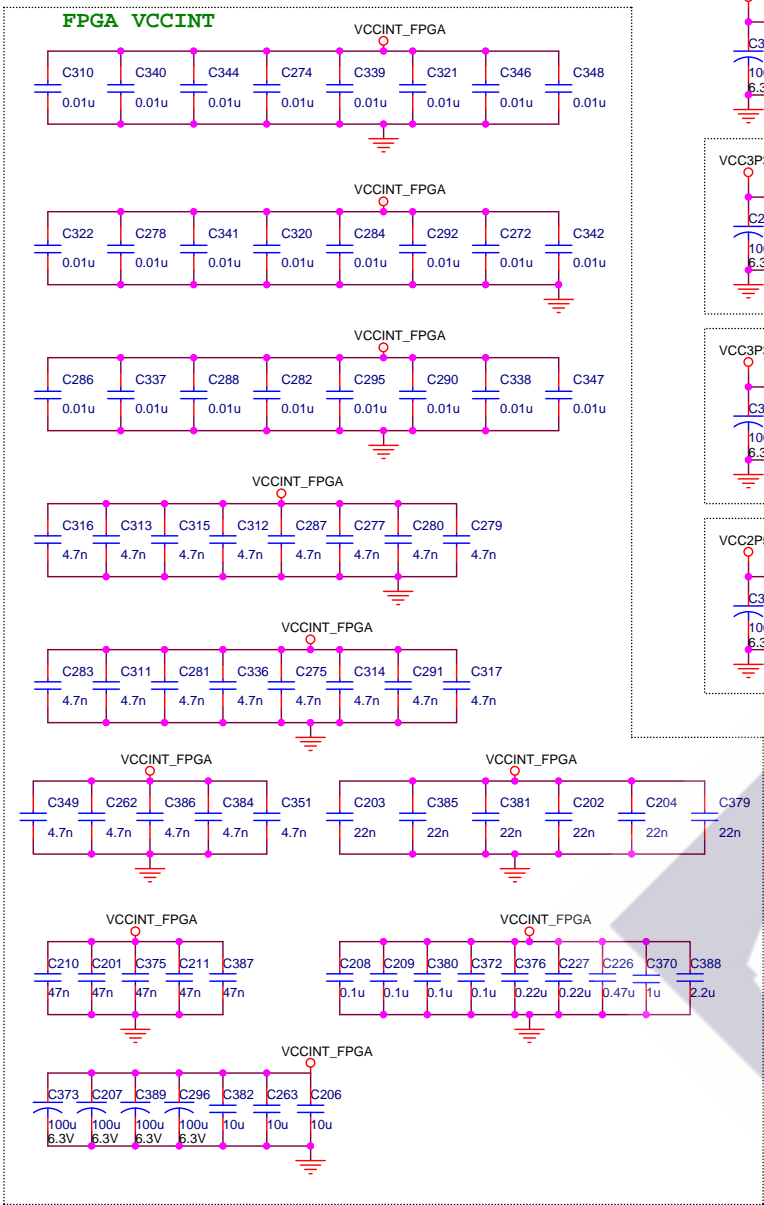


- R138 0 DNI MSEL0
- R137 0 DNI MSEL1
- R125 0 DNI MSEL2
- R124 0 DNI MSEL3
- R123 0 DNI MSEL4

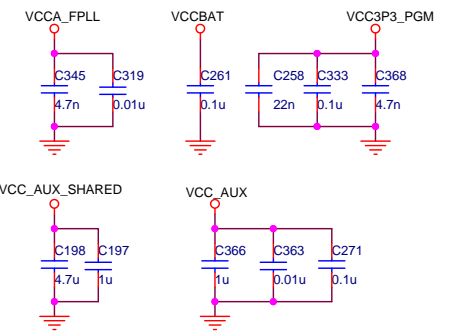
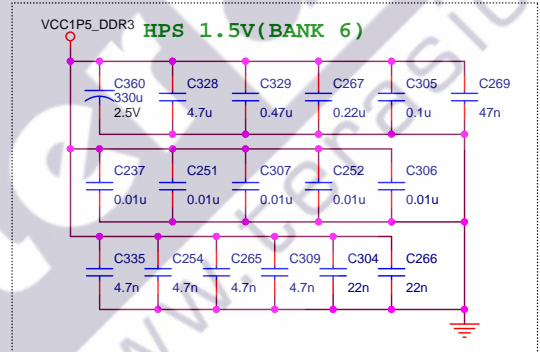
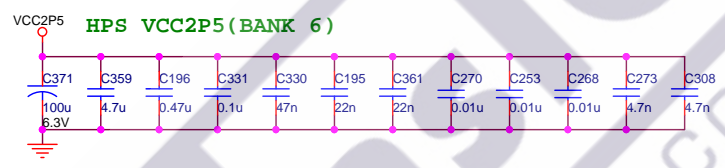
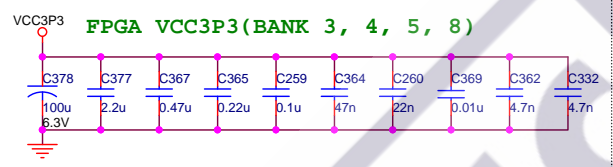


terasic Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

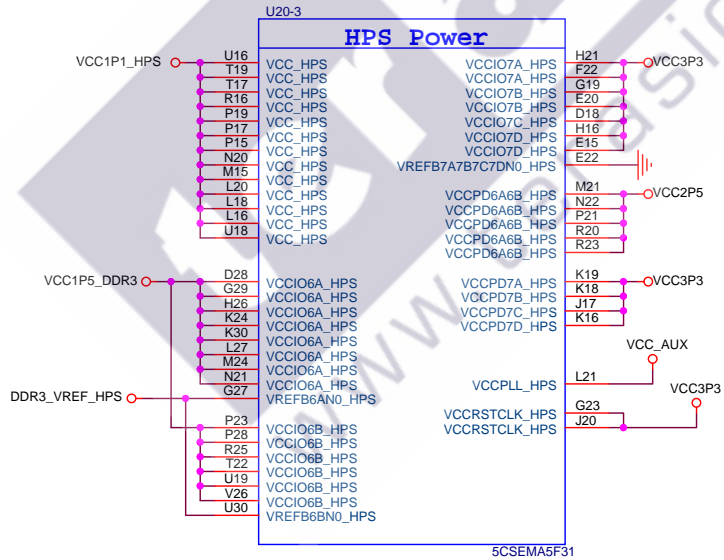
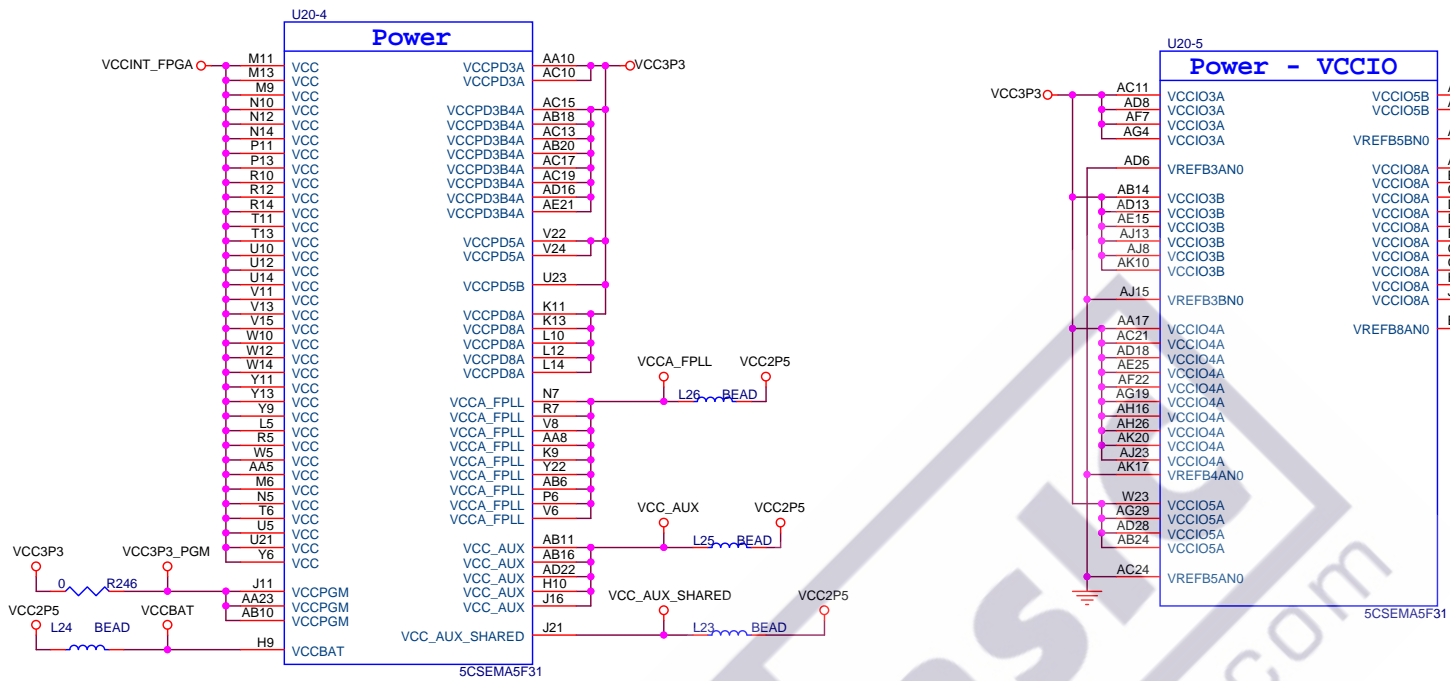
DE1-SoC Board		
Size B	Document Number FPGA Configuration	Rev E
Date:	Monday, October 20, 2014	Sheet 7 of 30




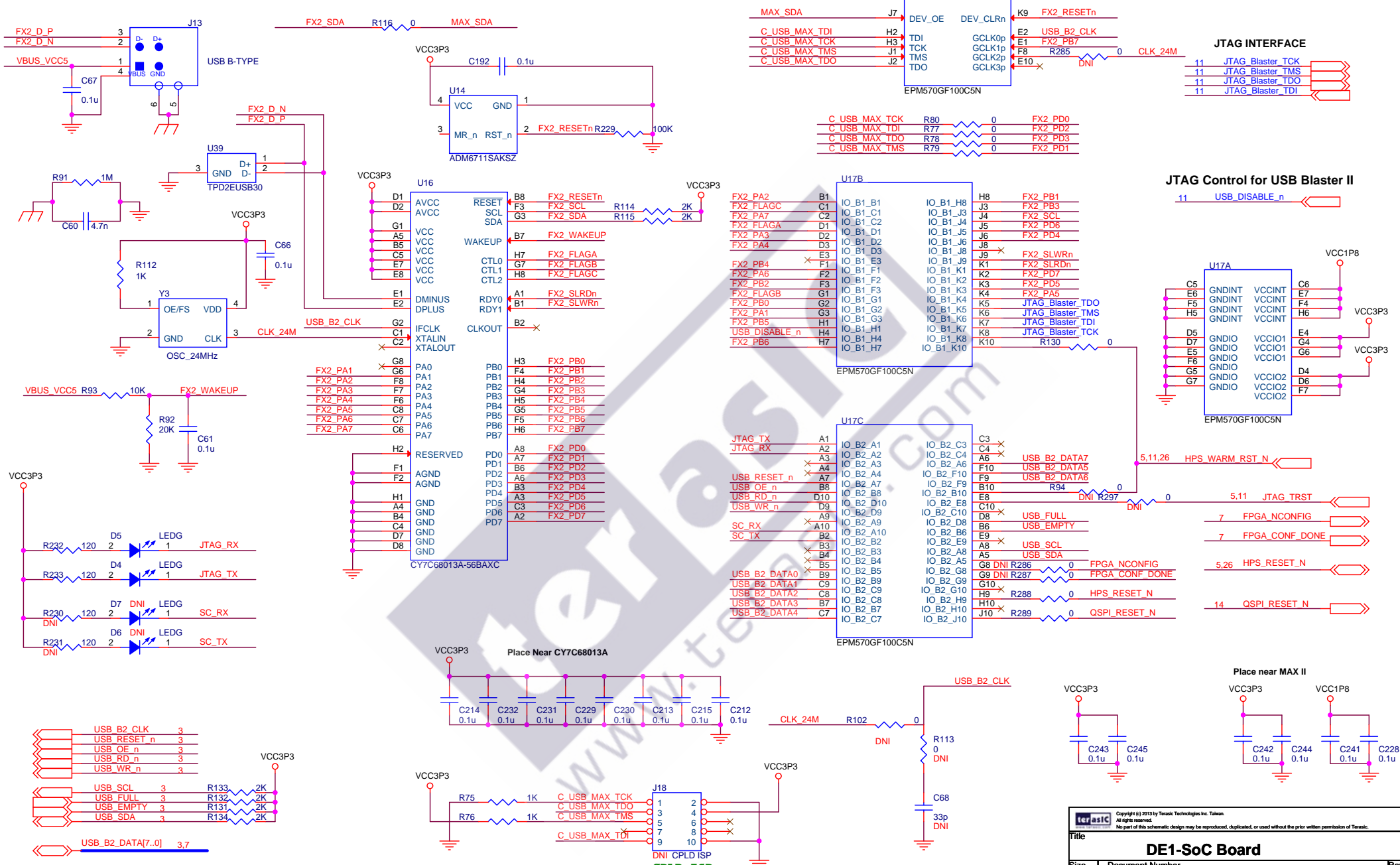
Place C394 close to J20/G23 pin



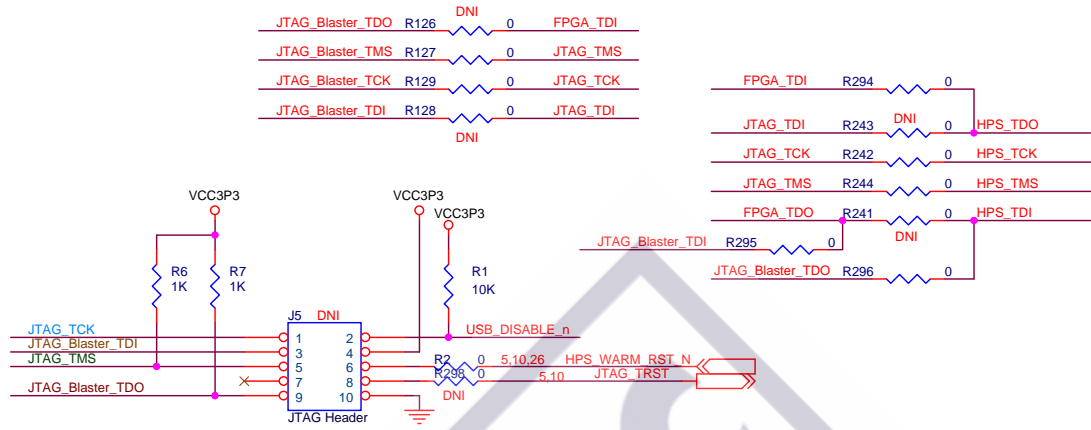
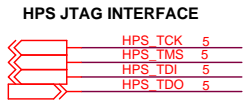
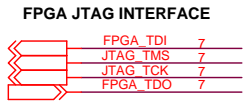
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size B	Document Number	Rev E
Date:	Monday, October 20, 2014	Sheet 8 of 30



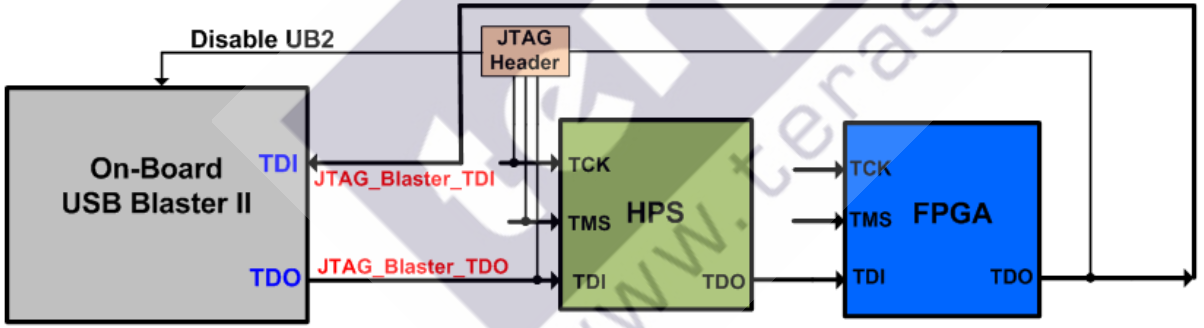
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	FPGA Power	E
Date:	Monday, October 20, 2014	Sheet 9 of 30

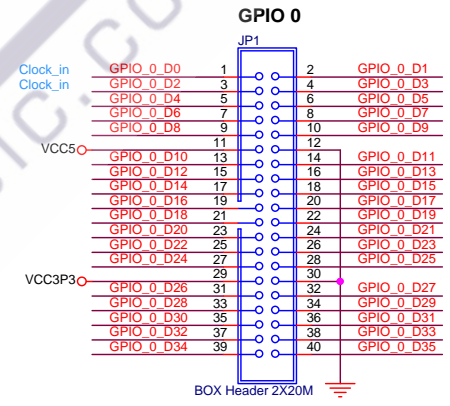
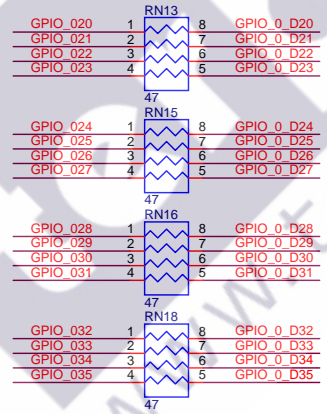
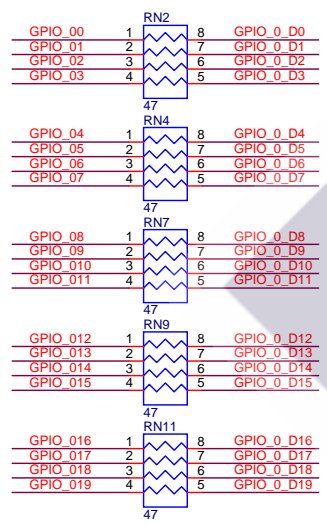
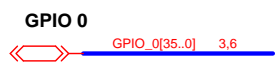
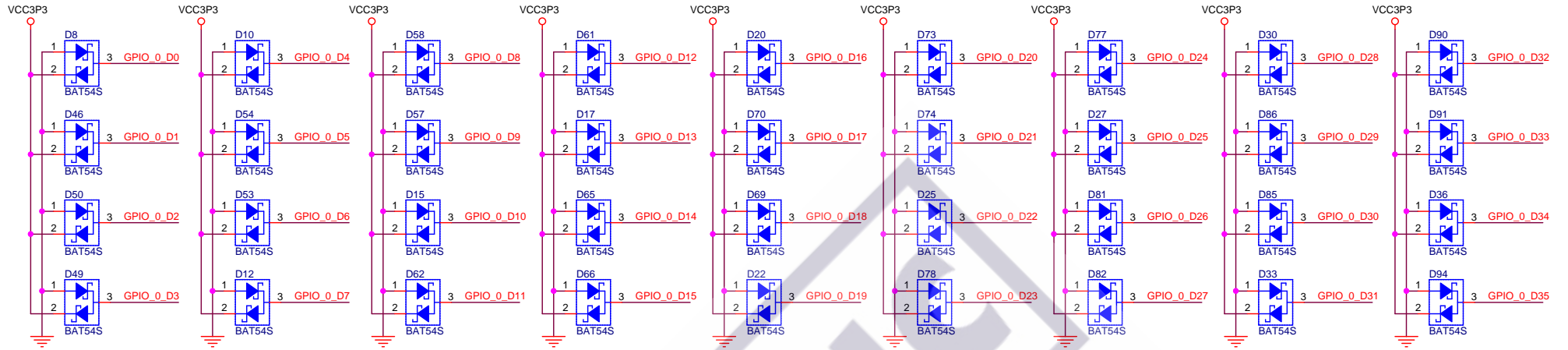


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title DE1-SoC Board		
Size B	Document Number USB Blaster II	Rev E
Date: Monday, October 20, 2014	Sheet 10 of 30	

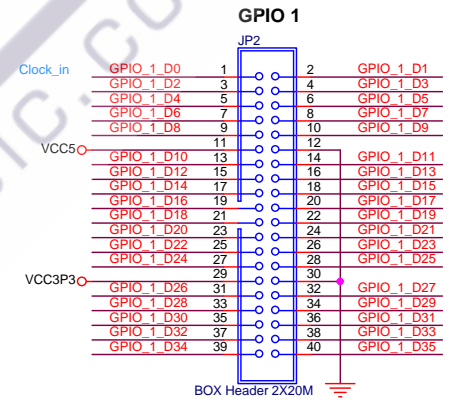
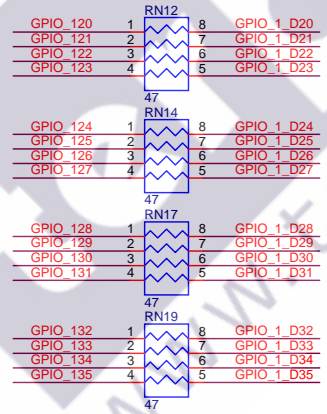
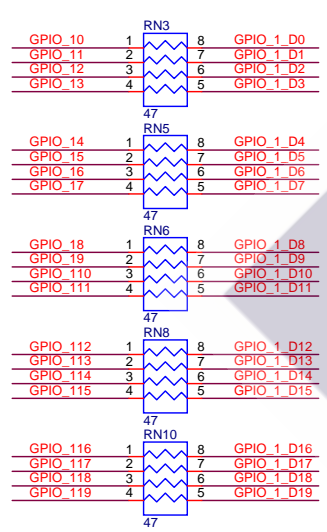
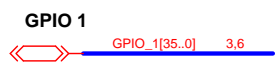
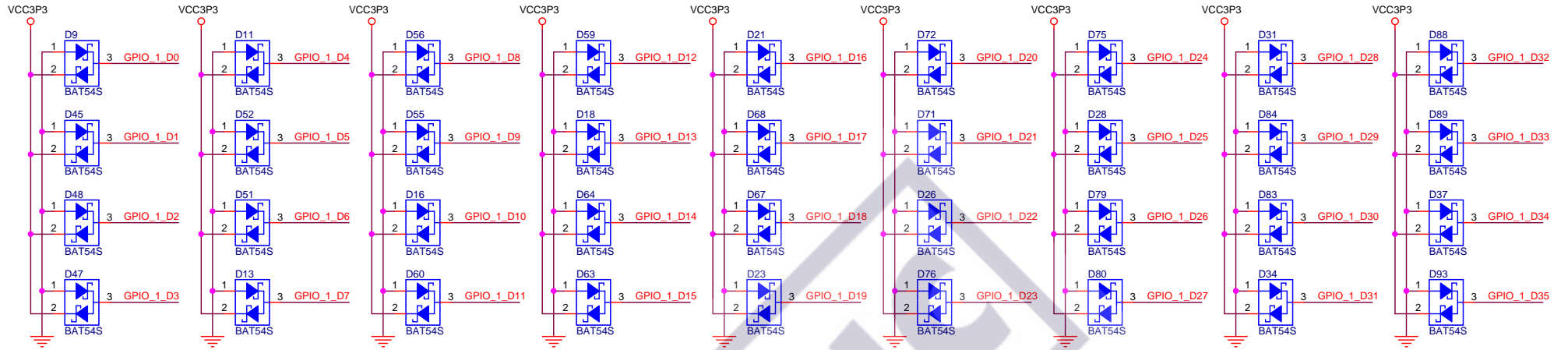


JTAG Chain

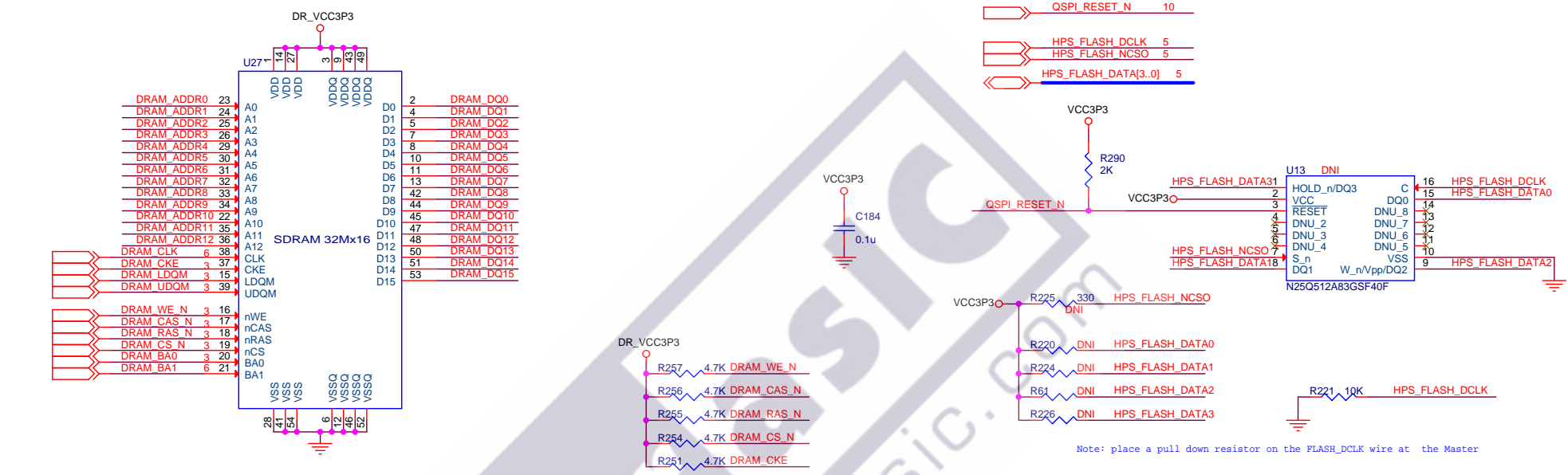




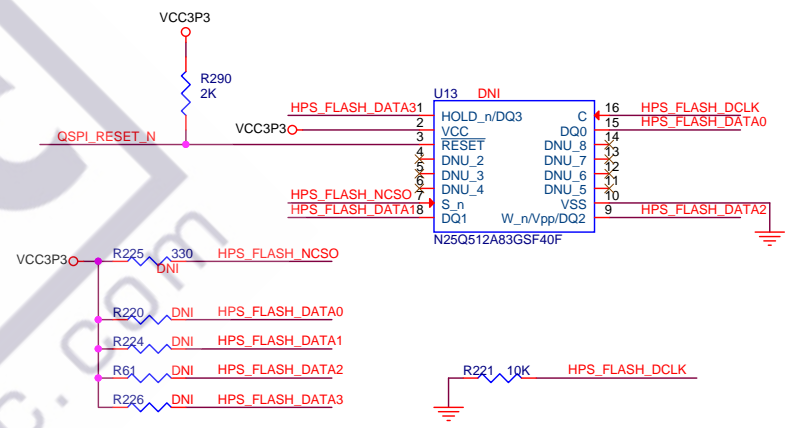
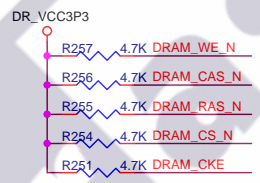
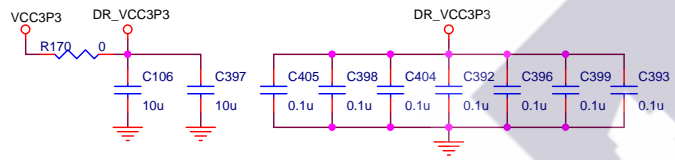
Title		
DE1-SoC Board		
Size B	Document Number	Rev E
GPIO 0		
Date:	Monday, October 20, 2014	Sheet 12 of 30

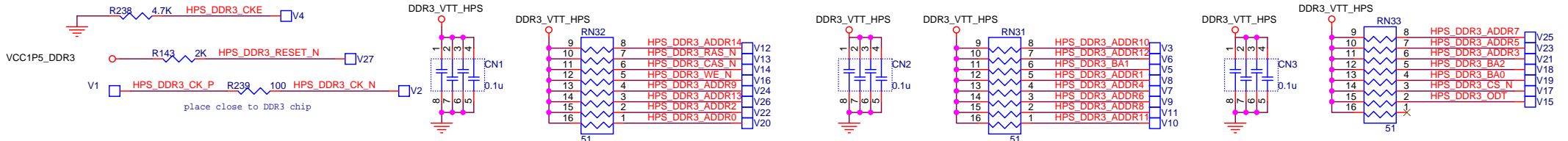


DRAM_DQ[15..0] 3
 DRAM_ADDR[12..0] 3,6

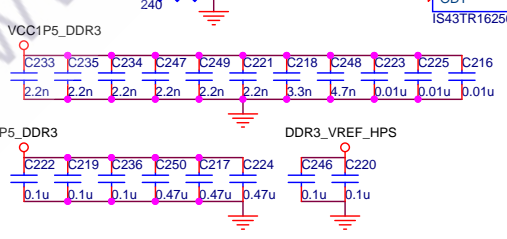
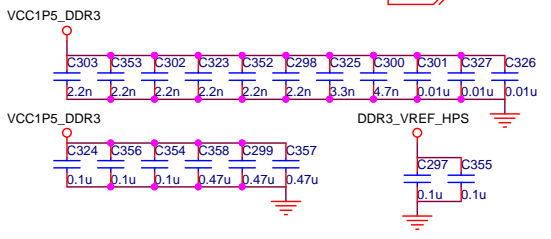
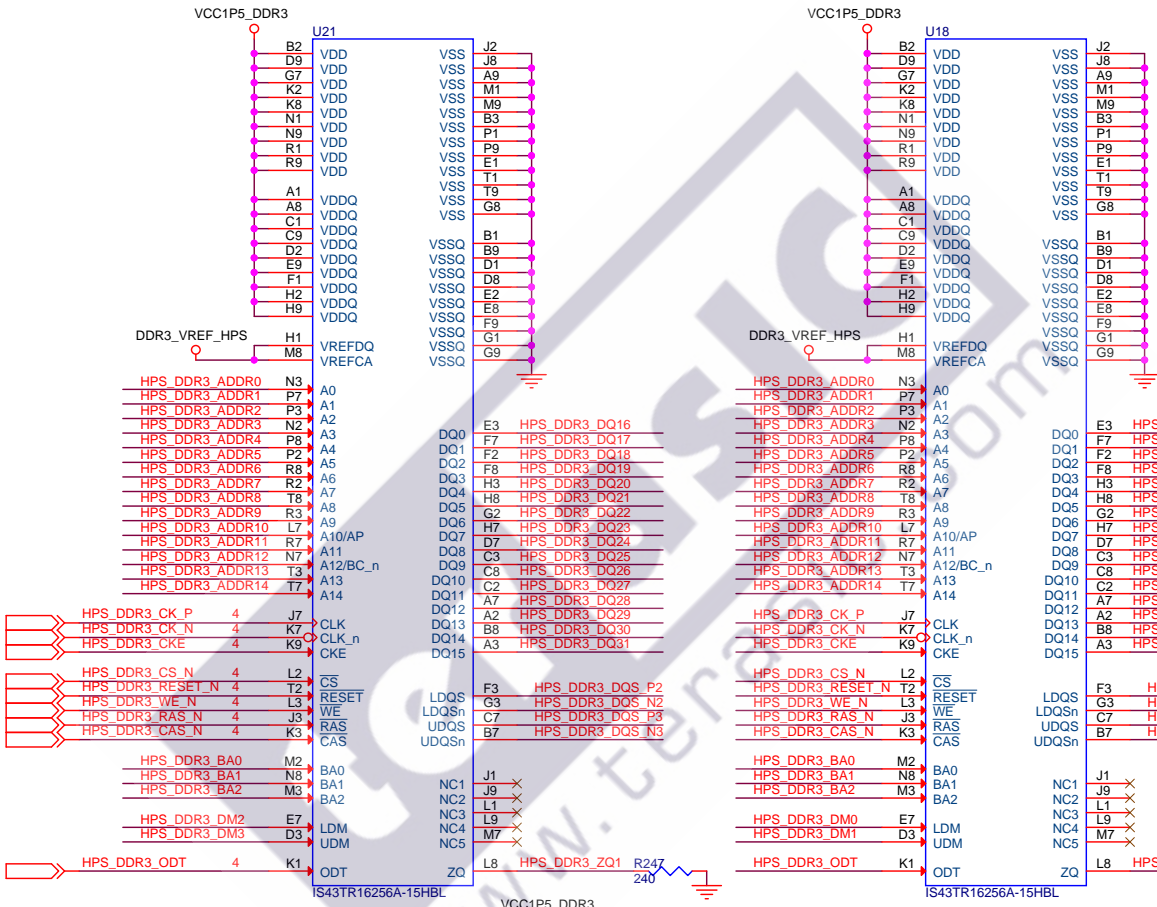
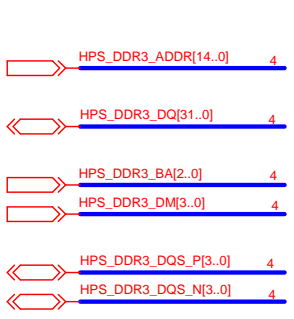


Note: place a pull down resistor on the FLASH_DCLK wire at the Master

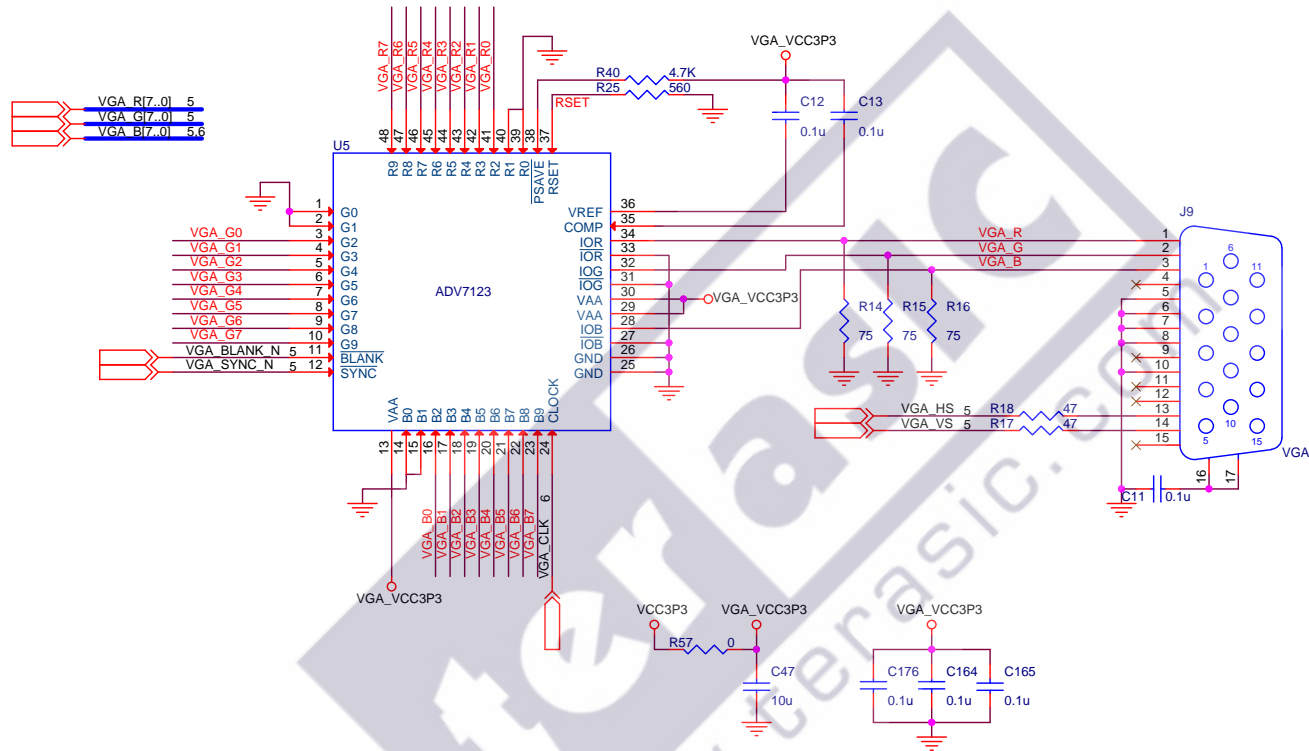





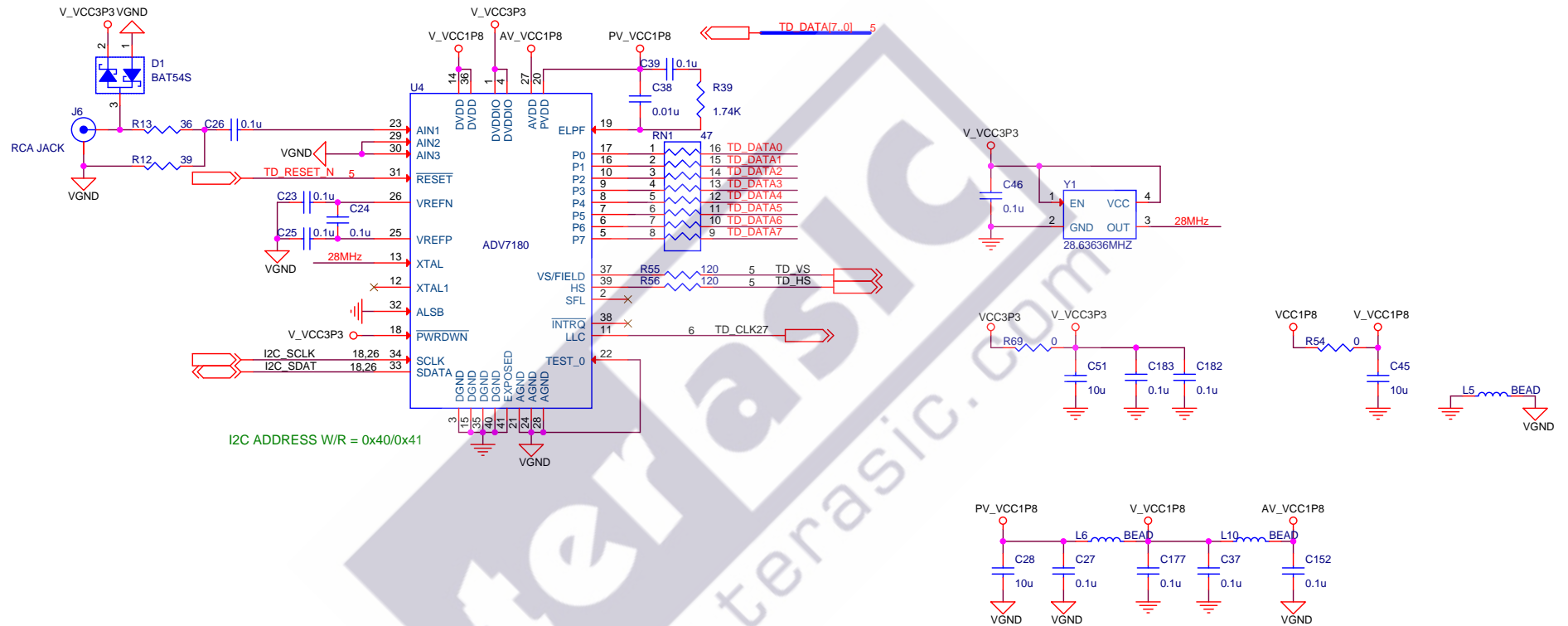
Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note: you can swap the signals on the OCT resistor array(include NC pin)



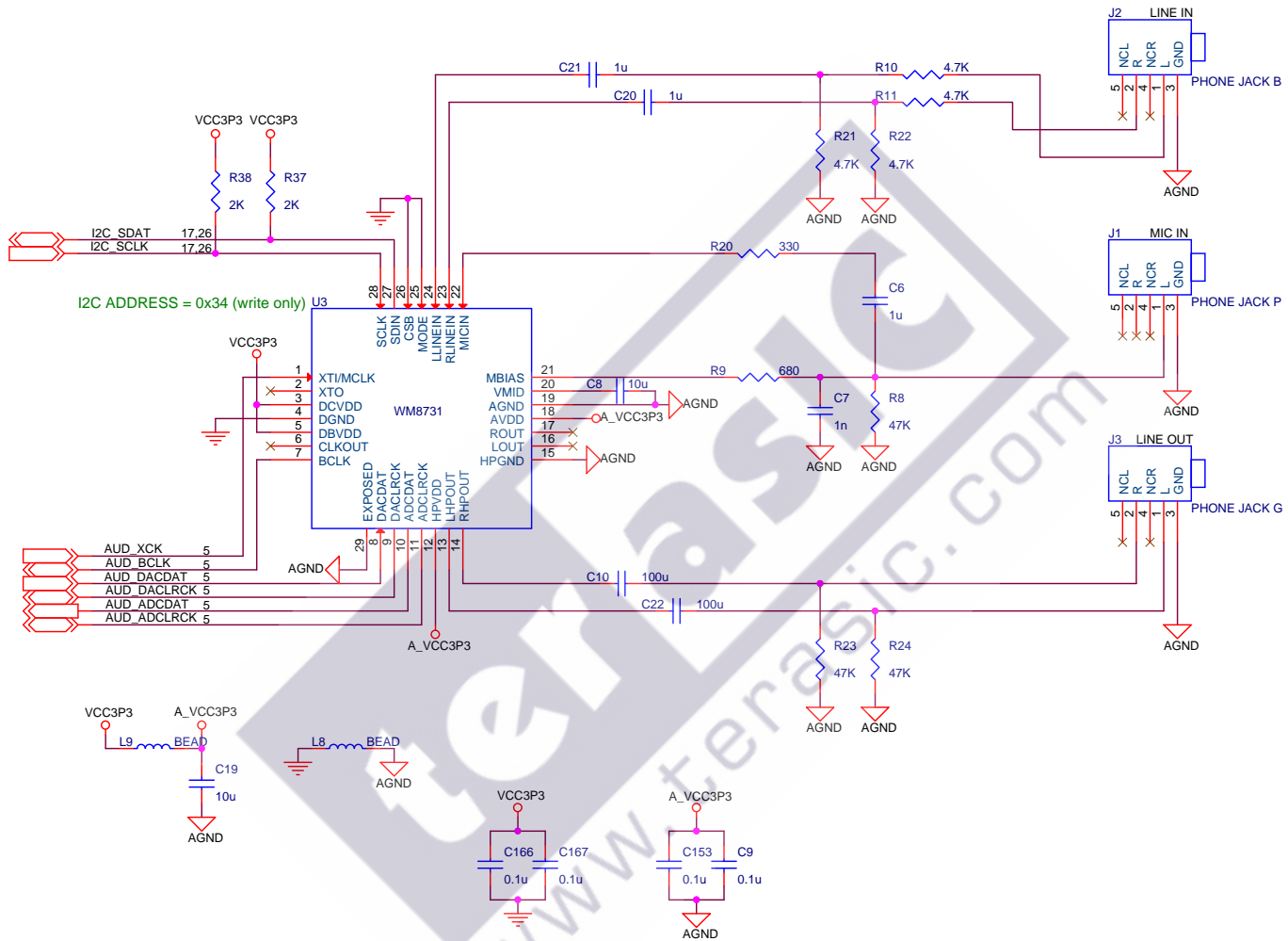
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	HPS DDR3 SDRAM	E
Date:	Monday, October 20, 2014	Sheet 15 of 30




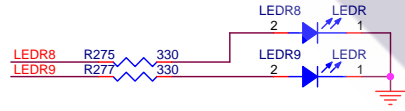
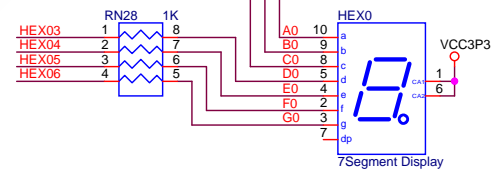
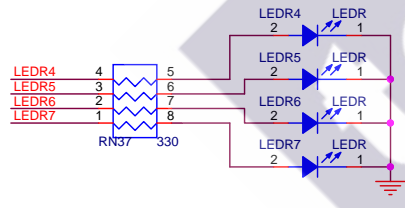
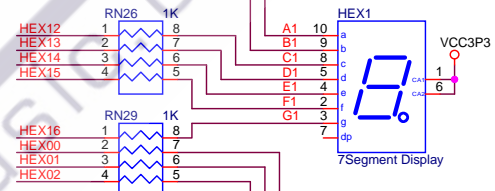
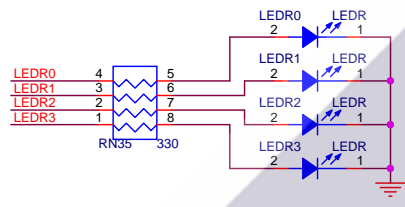
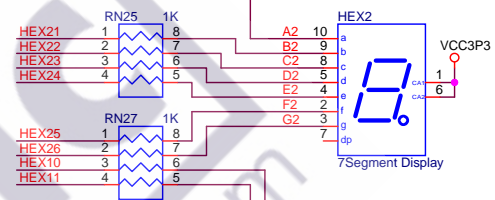
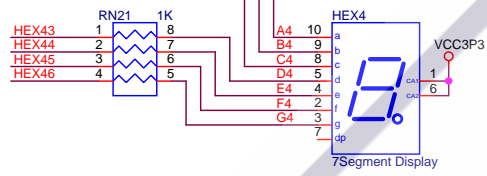
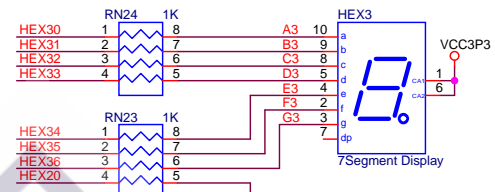
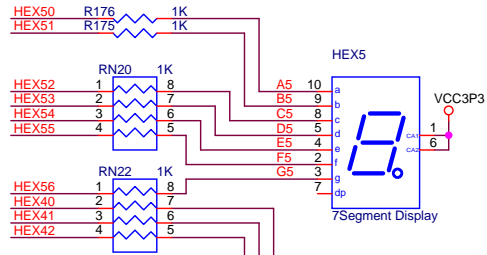
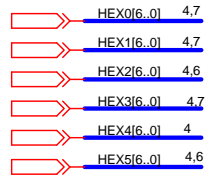
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	ADV7123 VGA	E
Date:	Monday, October 20, 2014	Sheet 16 of 30



Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size B	Document Number ADV7180 Video Decoder	Rev E
Date:	Monday, October 20, 2014	Sheet 17 of 30

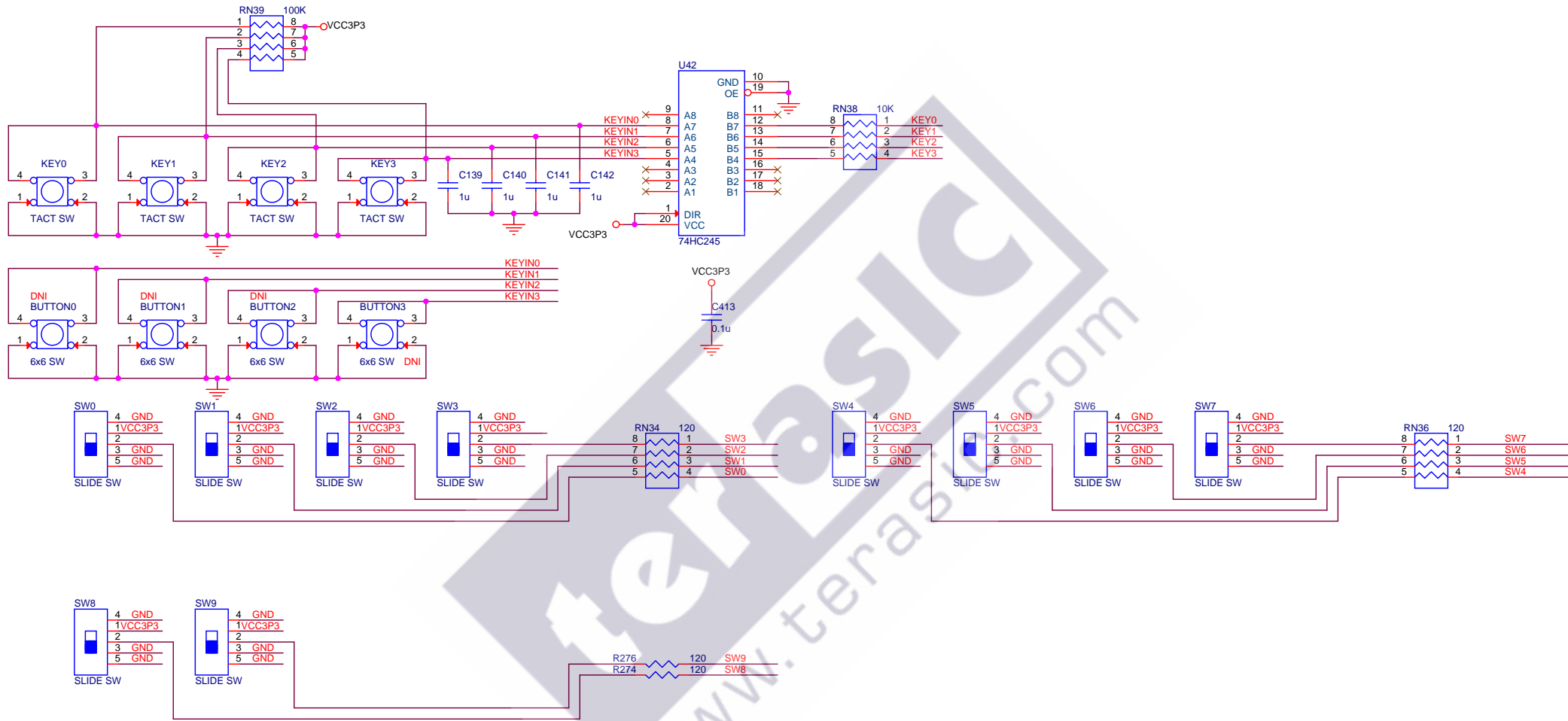


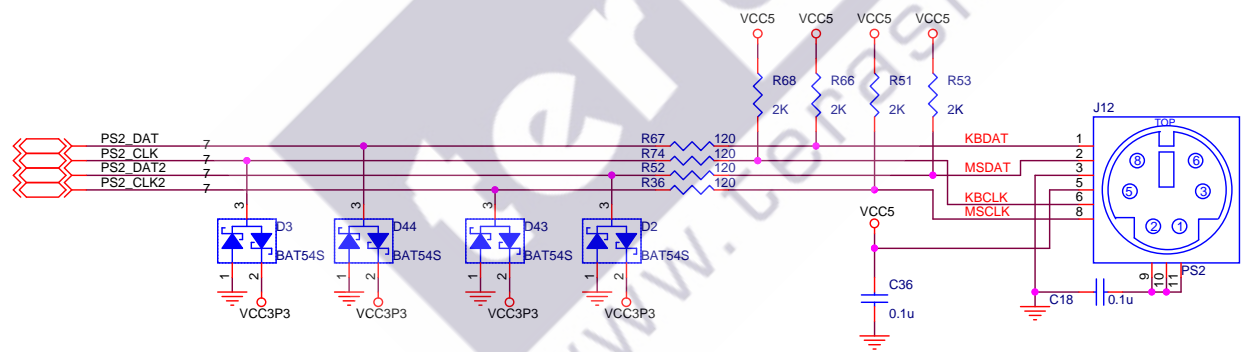
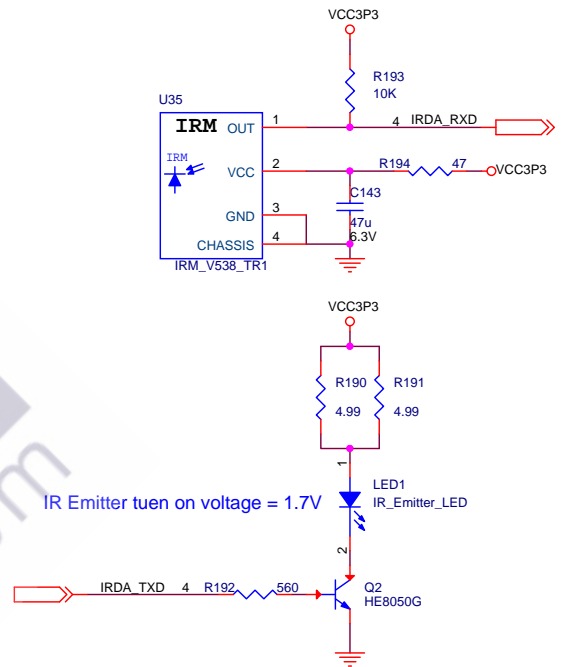
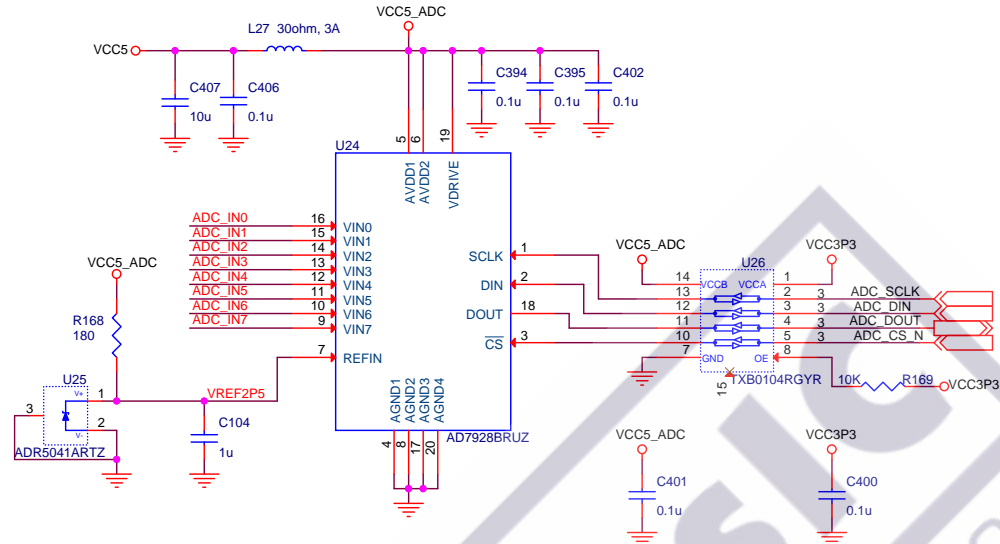
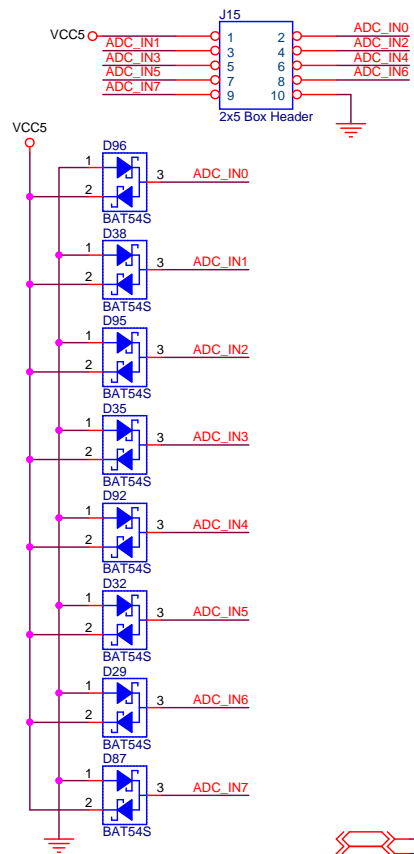
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
DE1-SoC Board	
Size	Document Number
B	Audio CODEC
Date:	Monday, October 20, 2014
Sheet	18 of 30
Rev	E



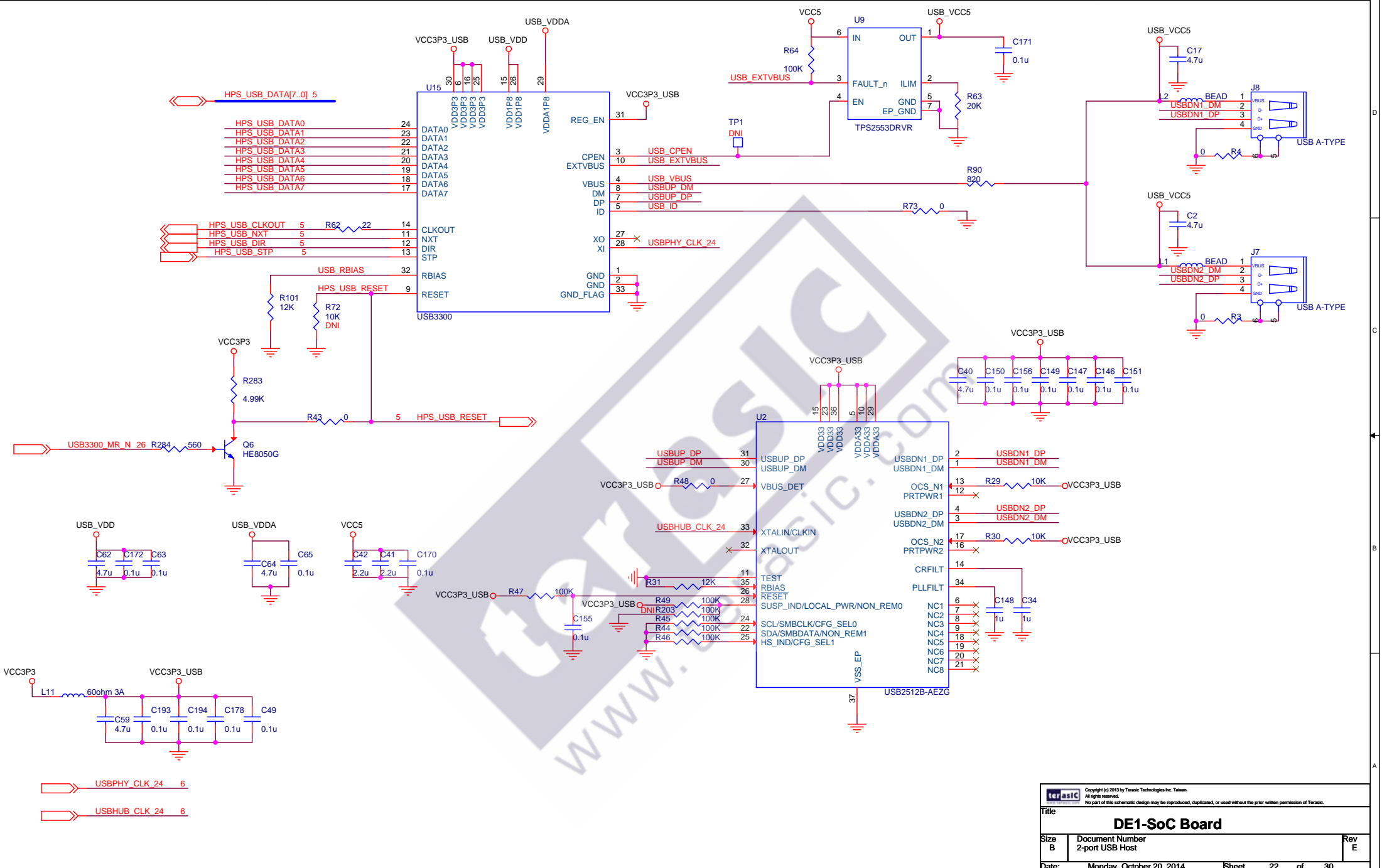
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	7-Segment Display, LED	E
Date:	Monday, October 20, 2014	Sheet 19 of 30

KEY[3..0] 3.6
 SW[9..0] 3.7

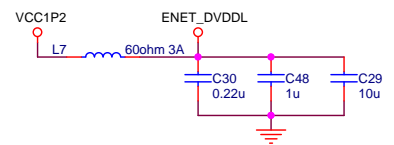
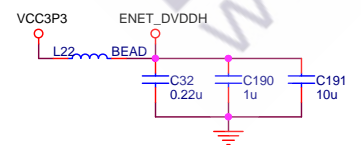
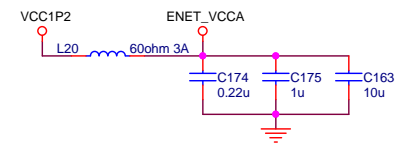
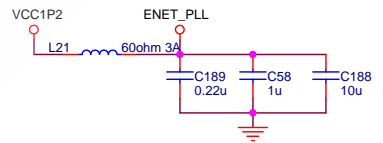
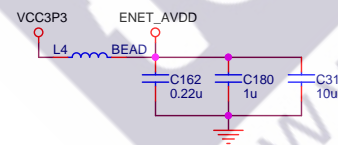
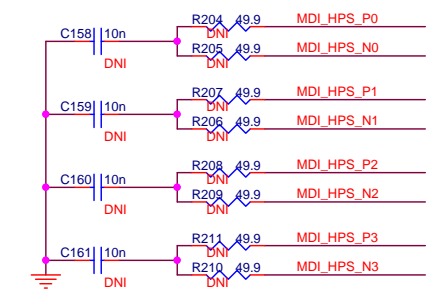
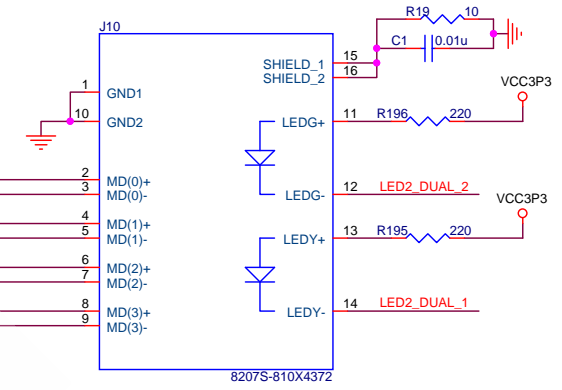
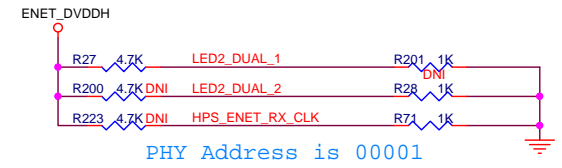
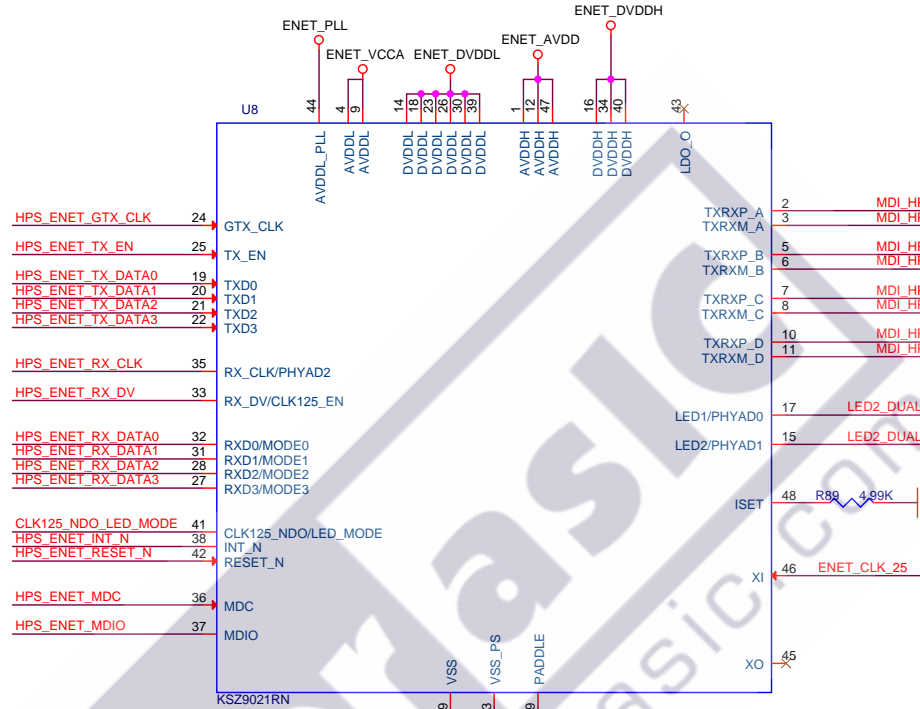
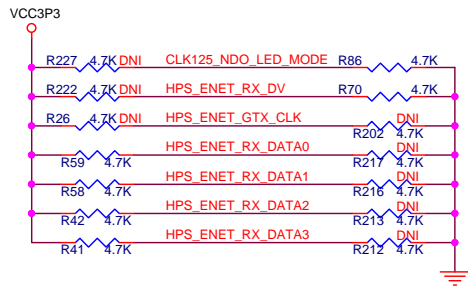
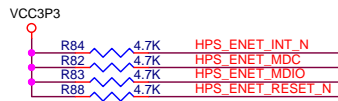
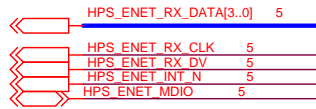
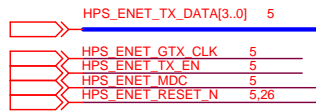




Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	ADC, PS2, IR Tx, IR Rx	E
Date:	Monday, October 20, 2014	Sheet 21 of 30

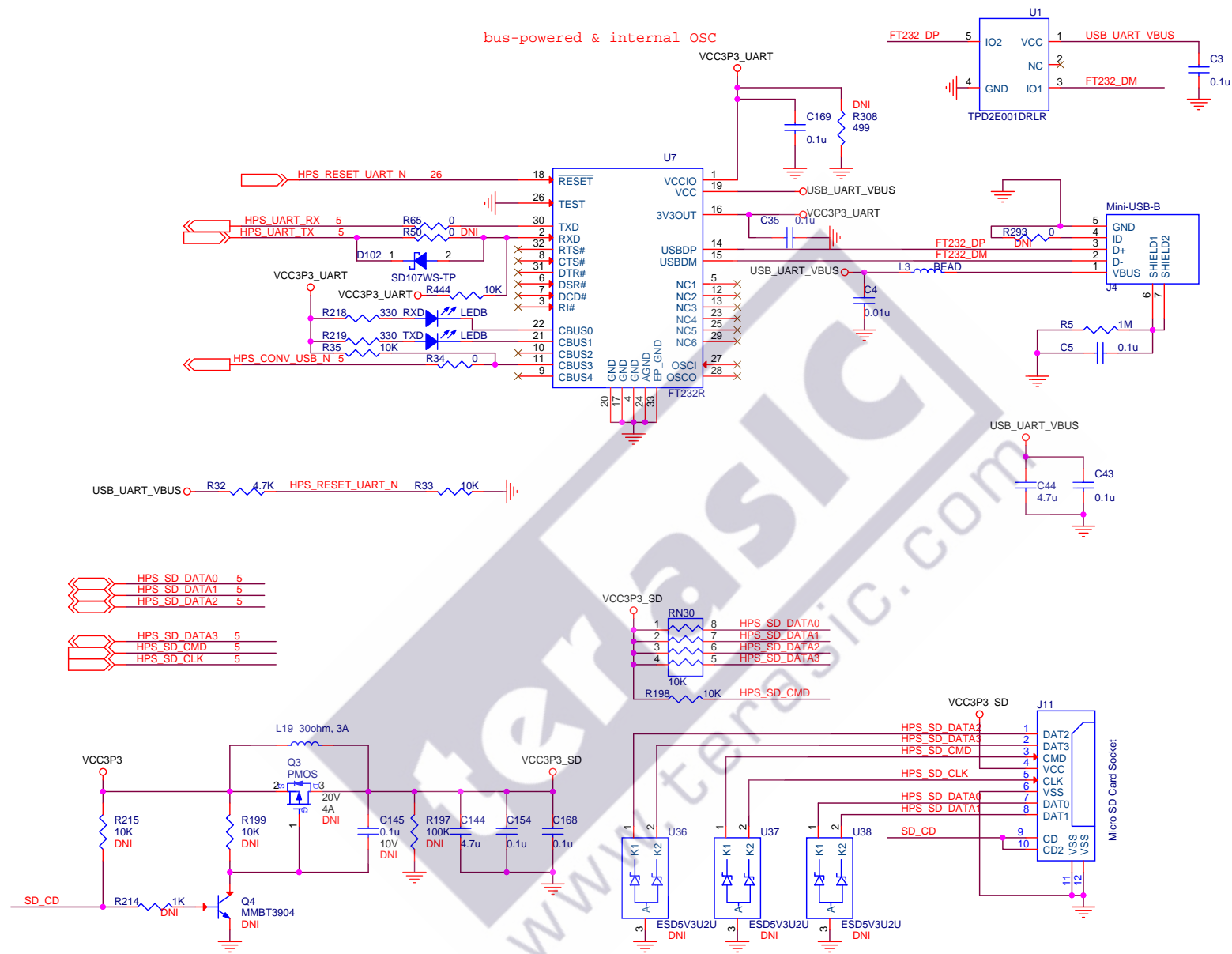


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	2-port USB Host	E
Date:	Monday, October 20, 2014	Sheet 22 of 30



icrstc Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

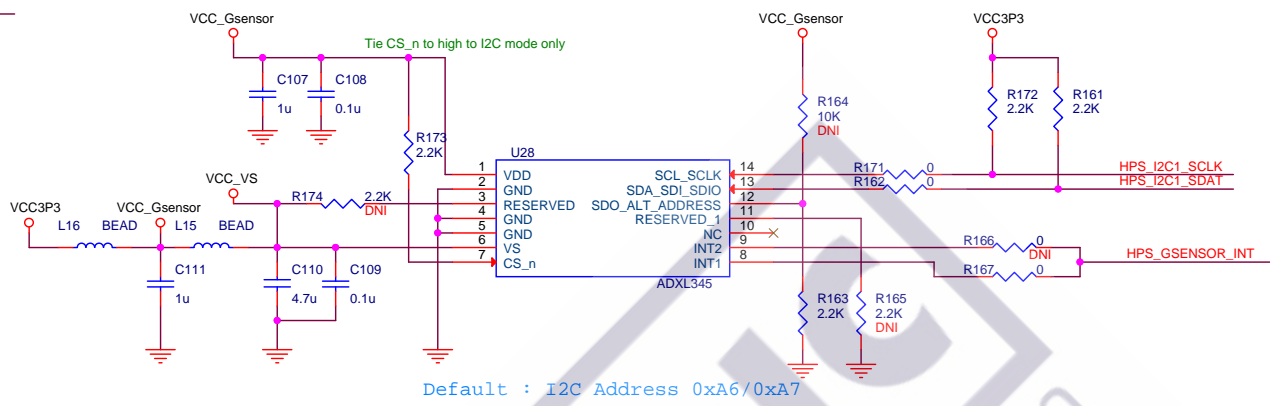
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	1	E
Date:	Monday, October 20, 2014	Sheet 23 of 30



Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	UART to USB, SD CARD	E
Date:	Wednesday, October 22, 2014	Sheet 24 of 30

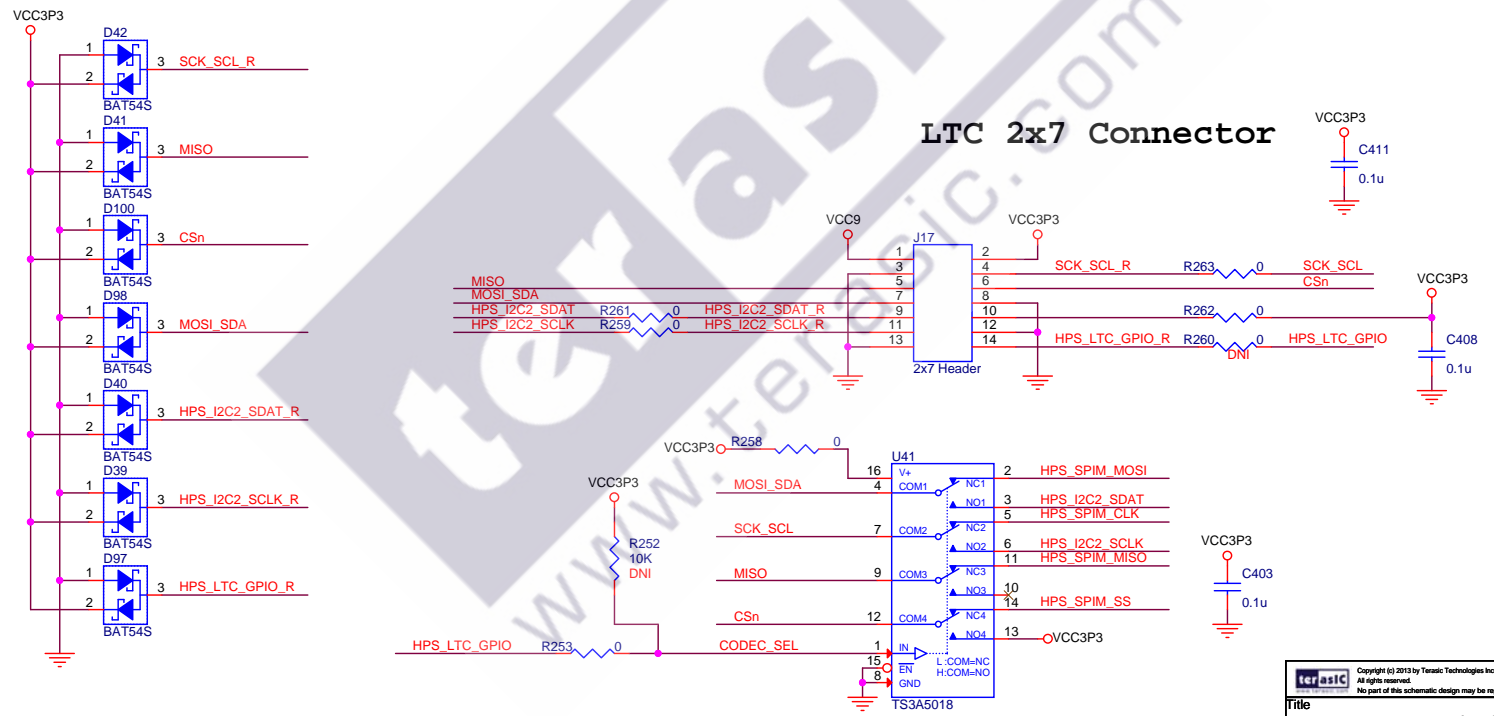
HPS_I2C1_SDAT 5,26
 HPS_I2C1_SCLK 5,26
 HPS_GSENSOR_INT 5

Digital Accelerometer



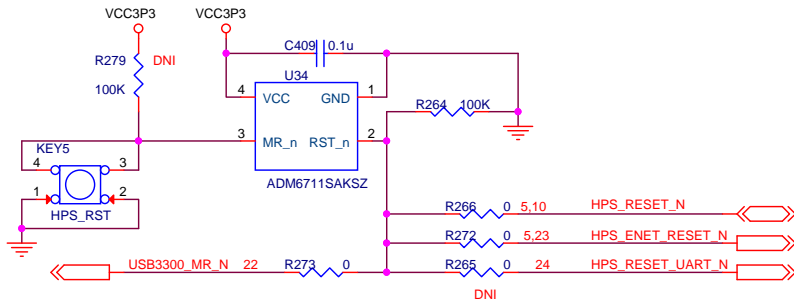
HPS_I2C2_SCLK 5
 HPS_I2C2_SDAT 5
 HPS_SPIM_MOSI 5
 HPS_SPIM_CLK 5
 HPS_SPIM_SS 5
 HPS_SPIM_MISO 5
 HPS_LTC_GPIO 5

LTC 2x7 Connector



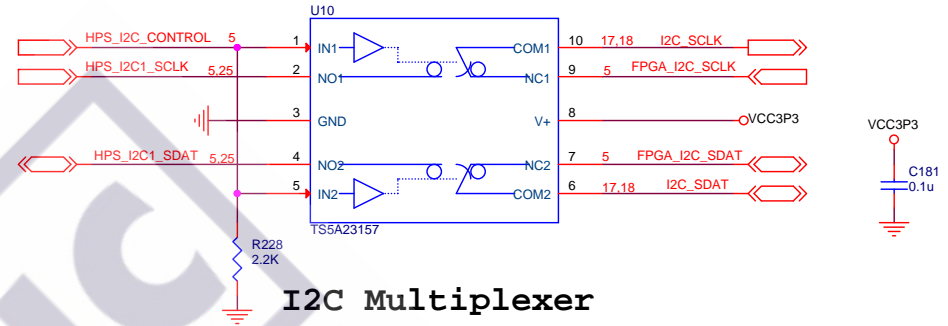
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
 All rights reserved.
 No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Accelerometer, LTC Connector	E
Date:	Monday, October 20, 2014	Sheet 25 of 30

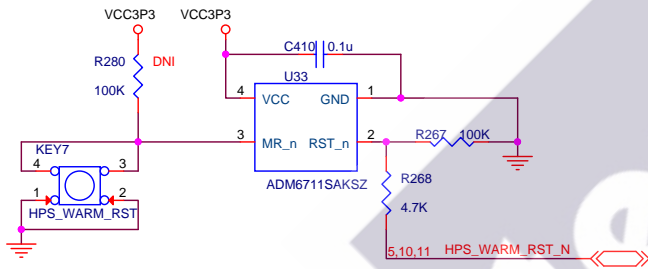


HPS Cold Reset

LOW --> NC to/from COM = ON and NO to/from COM = OFF
 HIGH --> NC to/from COM = OFF and NO to/from COM = ON



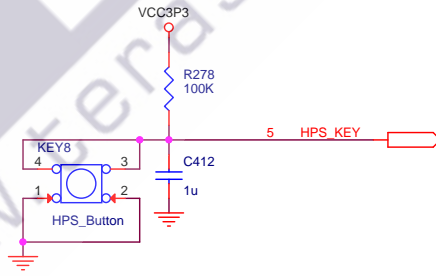
I2C Multiplexer




HPS Warm Reset

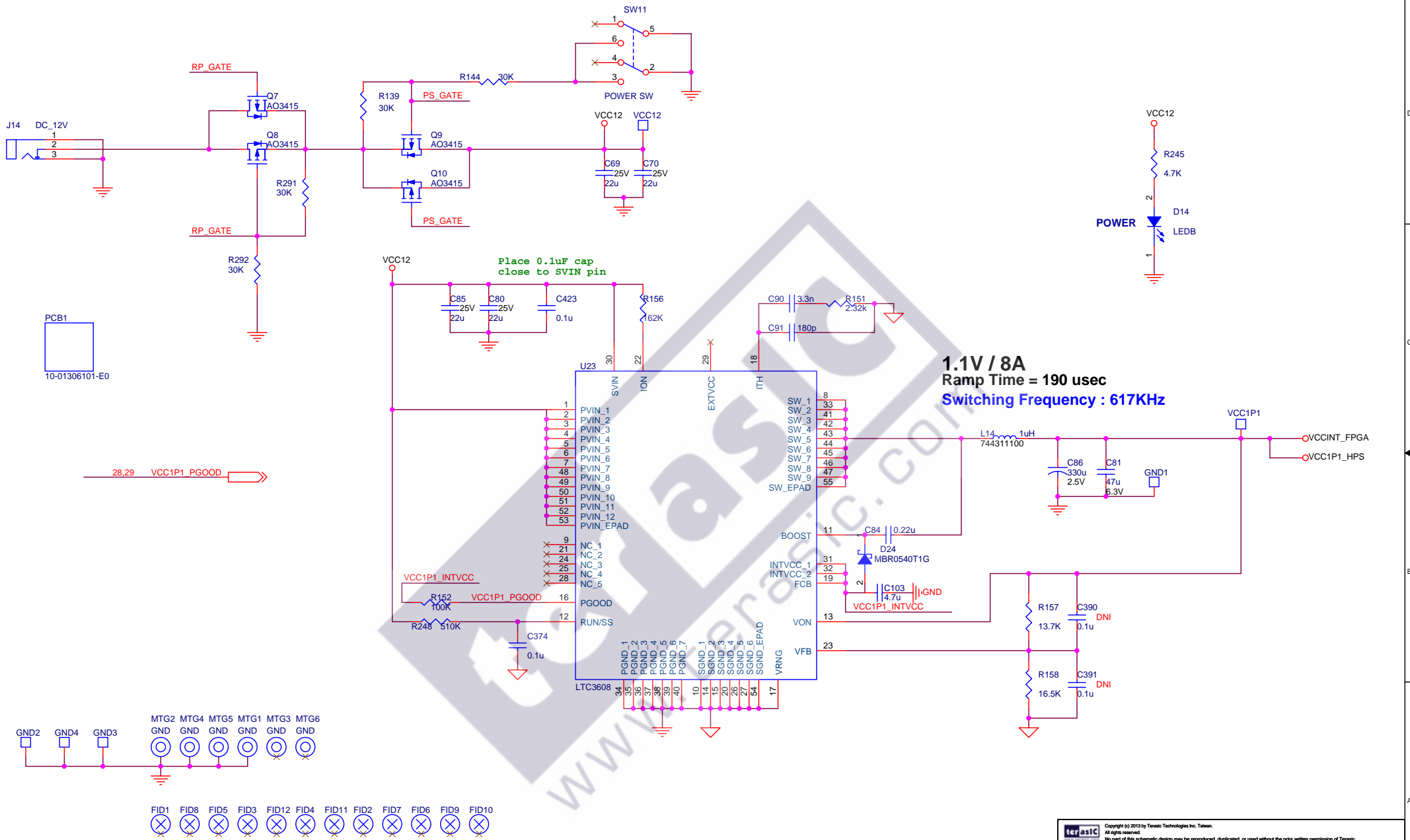


HPS User LED



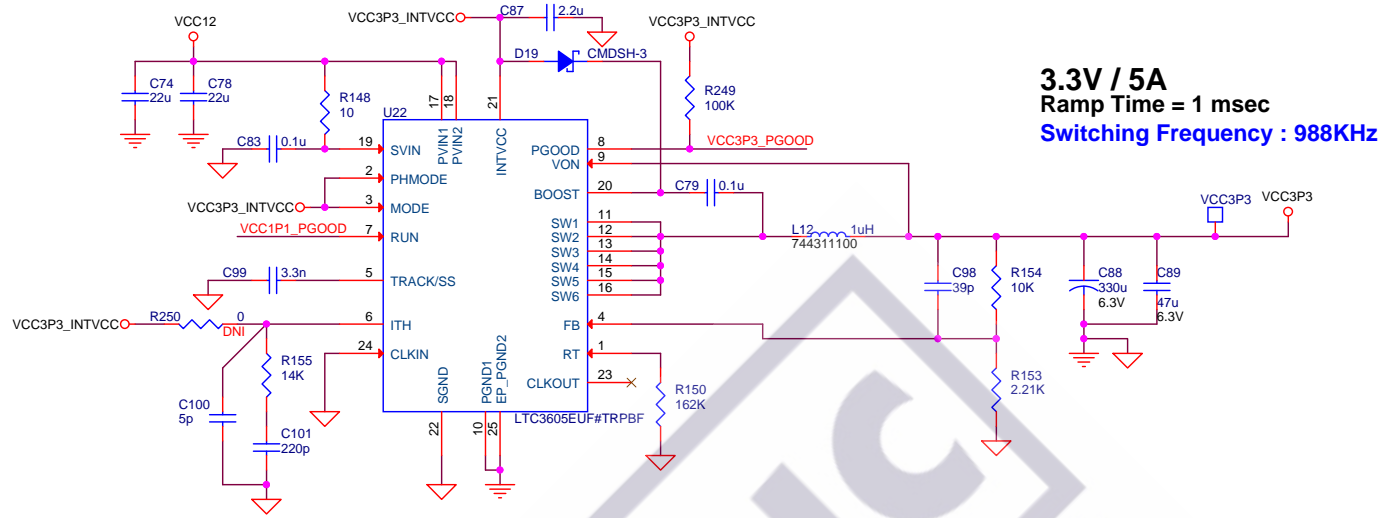
HPS User Button

 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	I2C Multiplexer, HPS BUTTON, HPS LED	E
Date:	Monday, October 20, 2014	Sheet 26 of 30

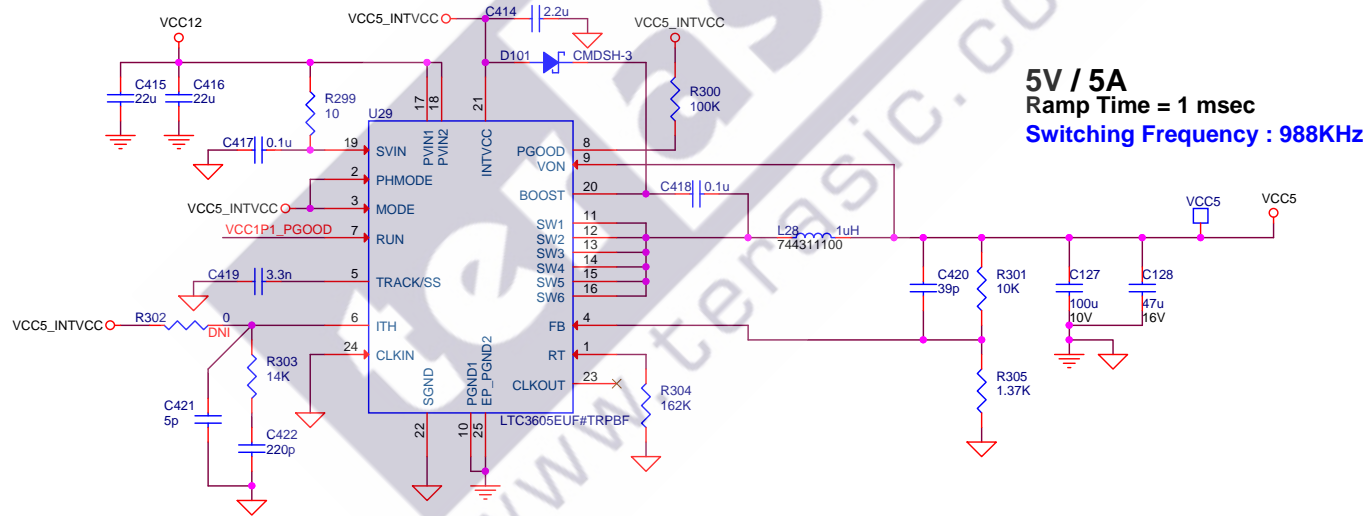


1.1V / 8A
Ramp Time = 190 usec
Switching Frequency : 617KHz

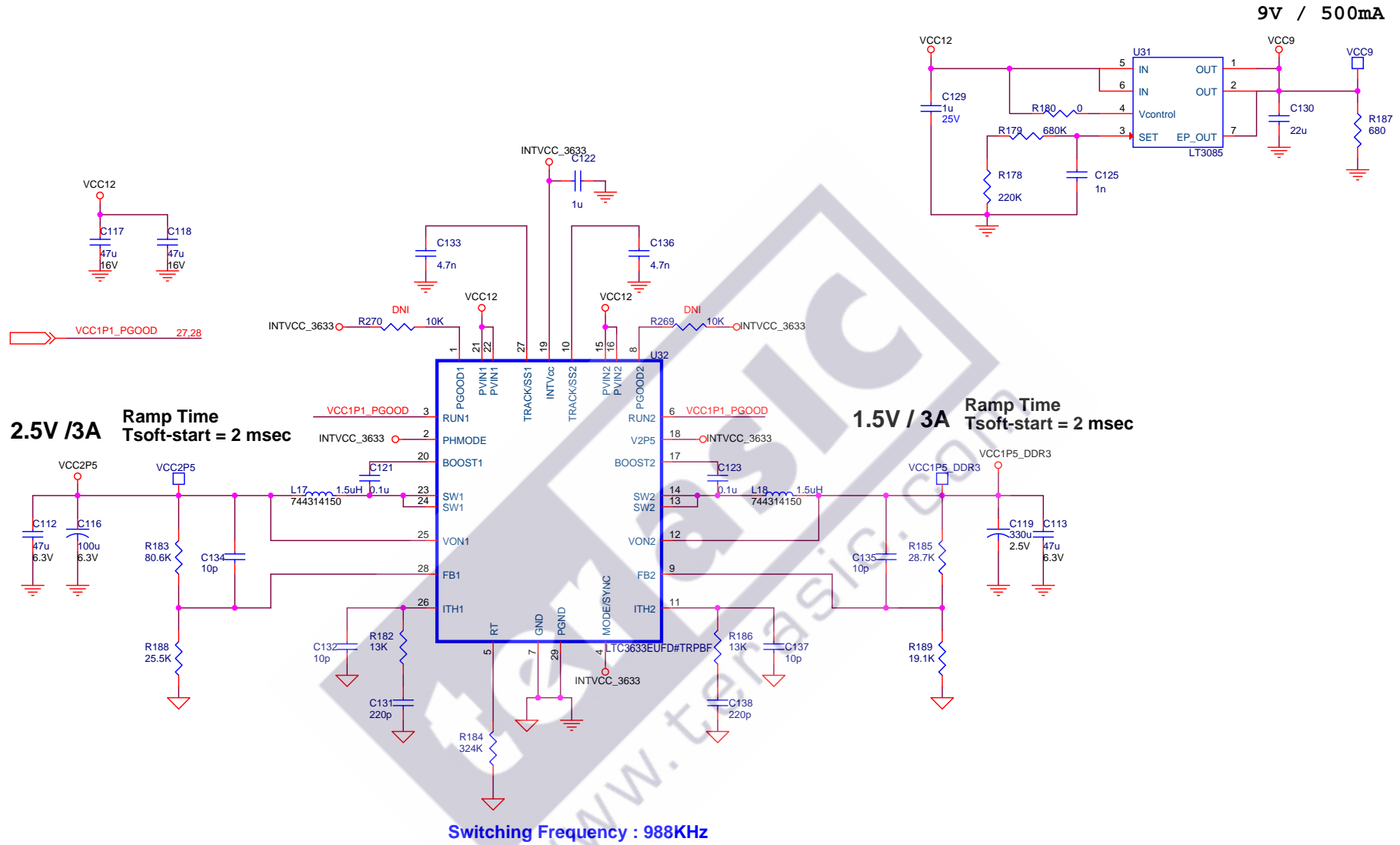
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size B	Document Number	Rev E
Power - 1.1V		
Date:	Monday, October 20, 2014	Sheet 27 of 30




VCC1P1_PGOOD 27,29

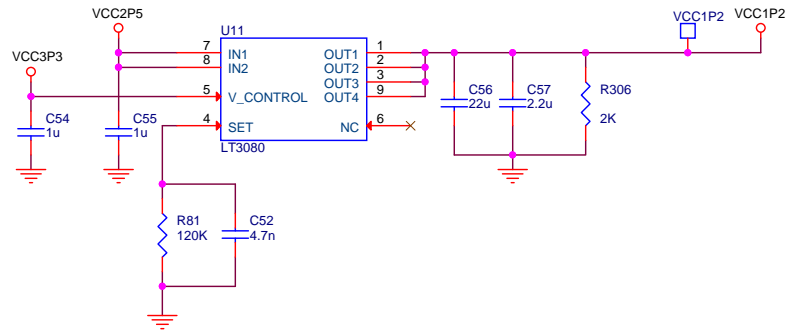


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Power - 5V, 3.3V	E
Date:	Monday, October 20, 2014	Sheet 28 of 30

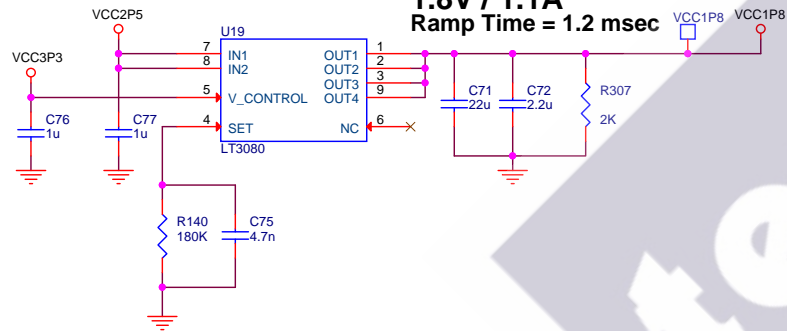


 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Power - 9V, 2.5V, 1.5V	E
Date:	Monday, October 20, 2014	Sheet 29 of 30

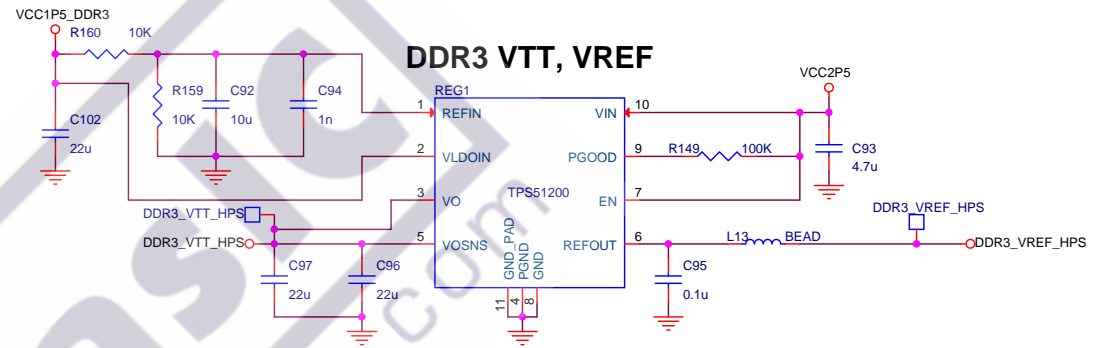
1.2V / 1.1A
Ramp Time = 0.8msec



1.8V / 1.1A
Ramp Time = 1.2 msec



DDR3 VTT, VREF



Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size B	Document Number	Rev E
Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT		
Date:	Monday, October 20, 2014	Sheet 30 of 30