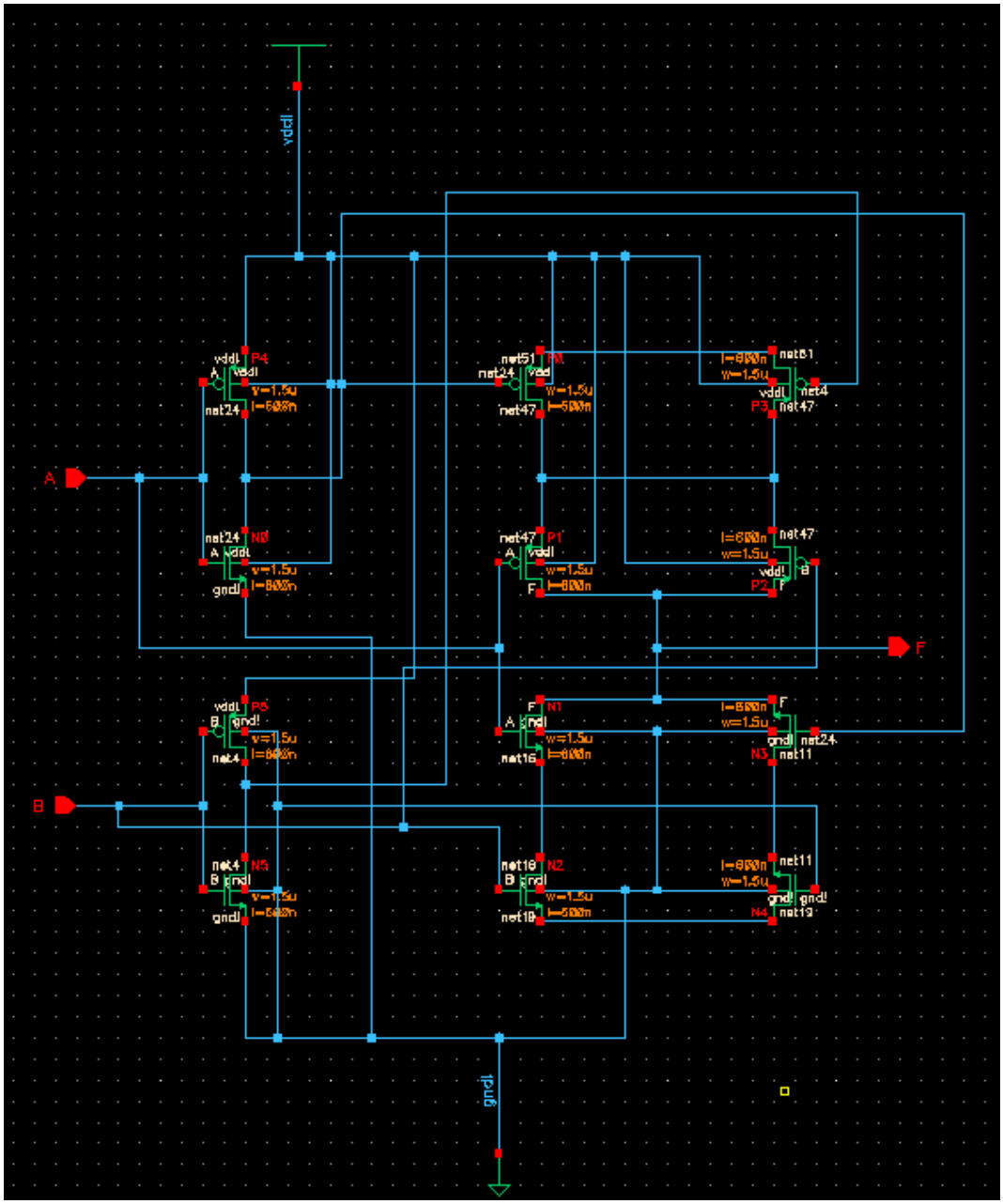
Guide to Drawing Clean Schematics with Virtuoso

A Cadence EDA Tools Help Document

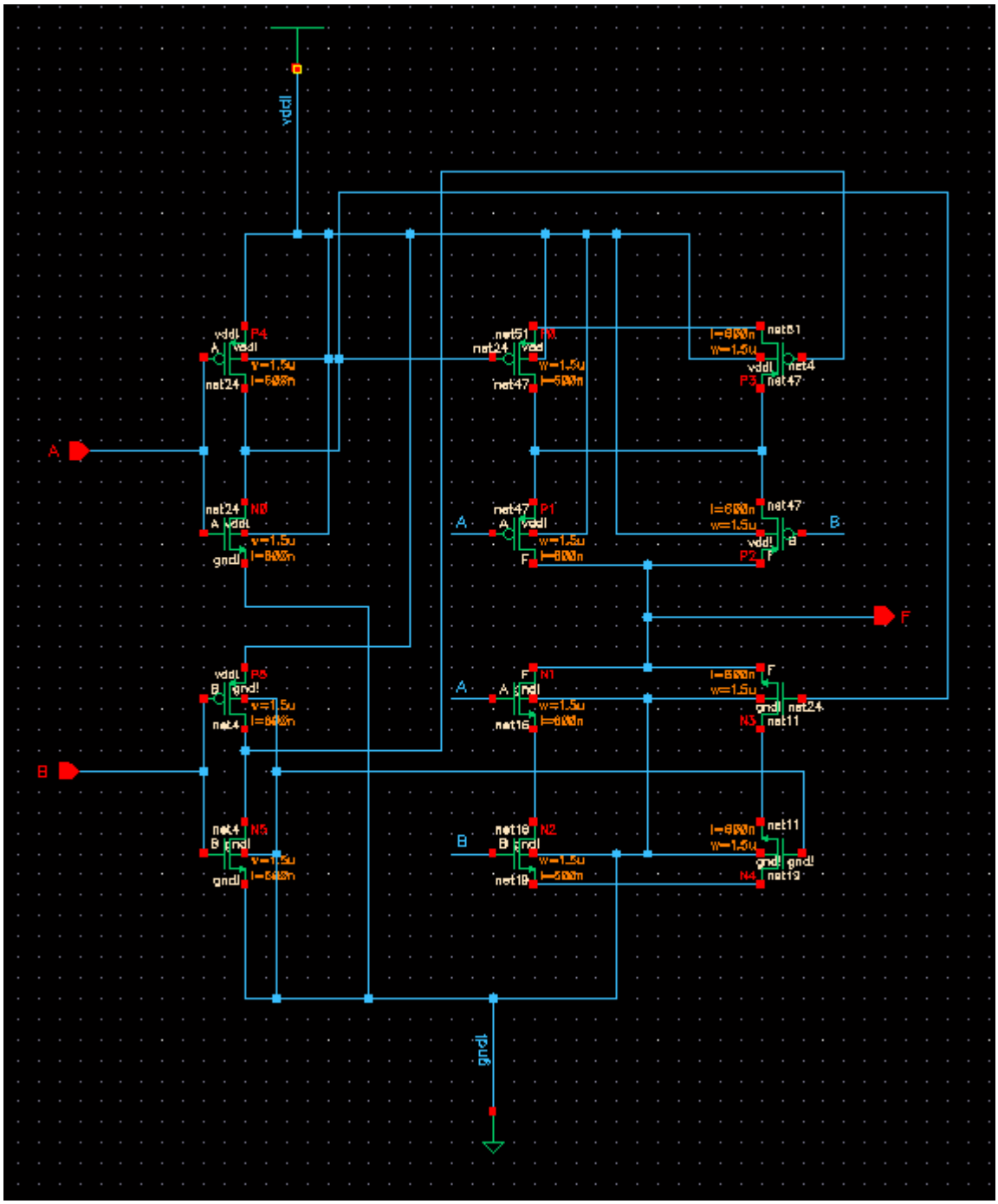
Created by Casey Wallace, Spring 2006

Shown in the figure below is an attempt at drawing an XOR schematic using Virtuoso schematic editor. The drawing is so unorganized that it is difficult to tell what circuit has actually been modeled. In addition, it contains at least five major wiring mistakes that are difficult to identify without a lengthy and careful examination. There are a few simple techniques that can be used to draw schematics that will vastly improve their readability, as well as make any wiring problems much easier to debug.



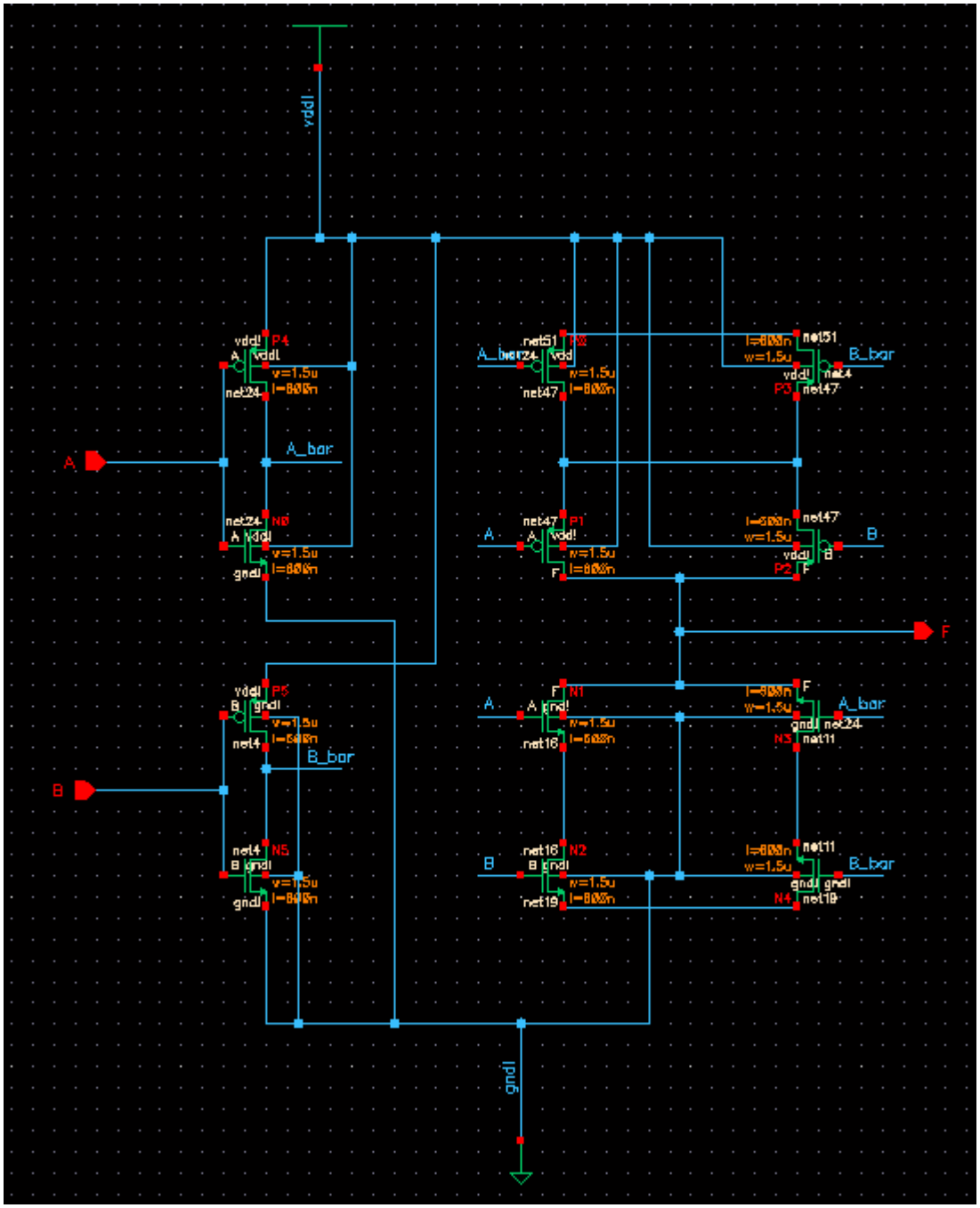
Tip #1: Net naming using primary input pins

Any net (i.e. wire) connected to a pin is automatically given the name of the pin. Additionally, any net given the same name as a pin becomes connected to that pin. Therefore, you can replace much of the wiring from pin connections, and eliminate the using of multiple pins with an identical name by utilizing net naming. You can add a label to a wire by pressing ‘l’, entering the name of the label, and then clicking on the wire.



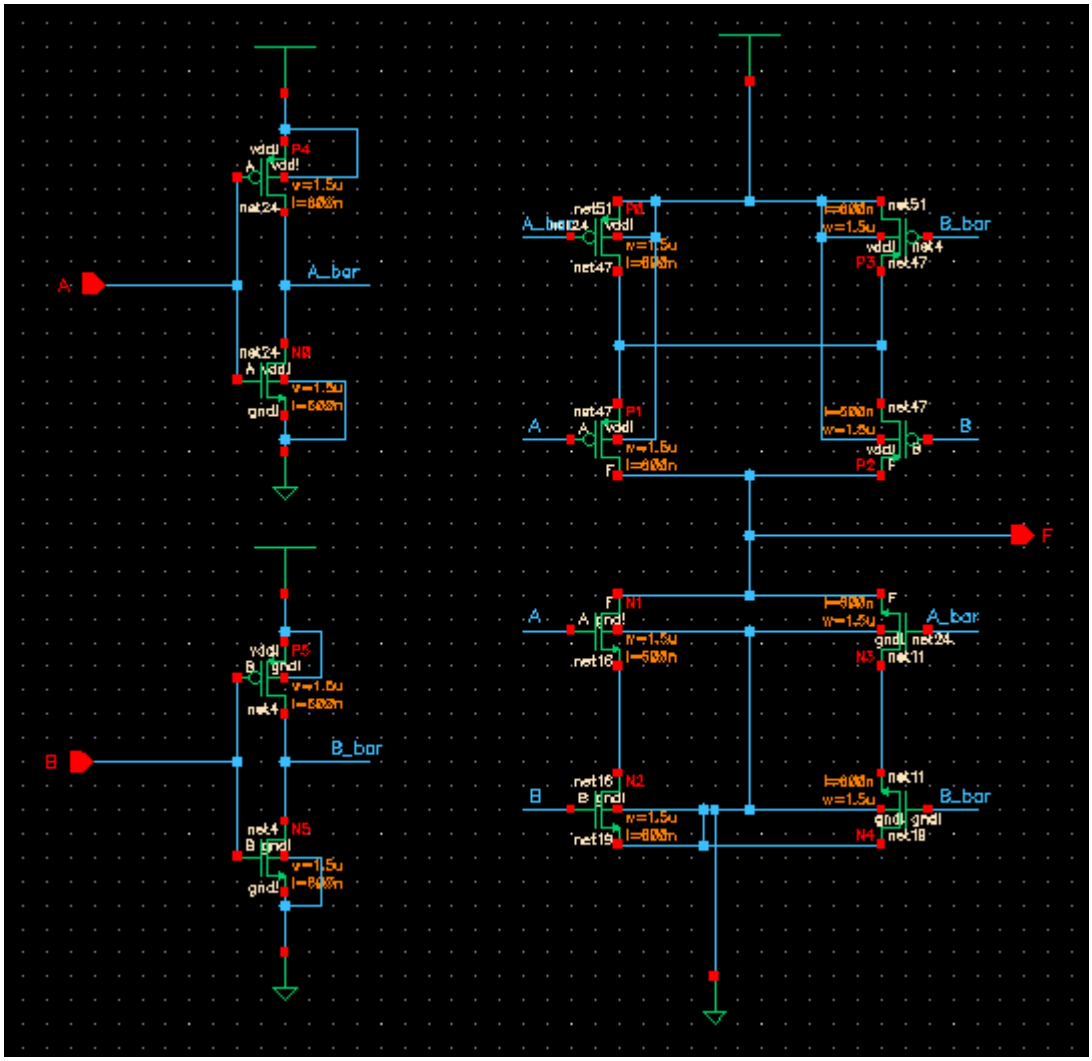
Tip #2: Net naming intermediate nets

In order to connect two nets together, you may label them with the same name. If the wire is not connected to a primary input, output, or supply net in the schematic (i.e. an intermediate net), you may give the wire any name you wish. In the figure below, the inverter output nets are named. All transistors' gate terminals connected to these inverter outputs are connected to a short wire and given the same name. All nets sharing the same name indicate a shared electrical connection.



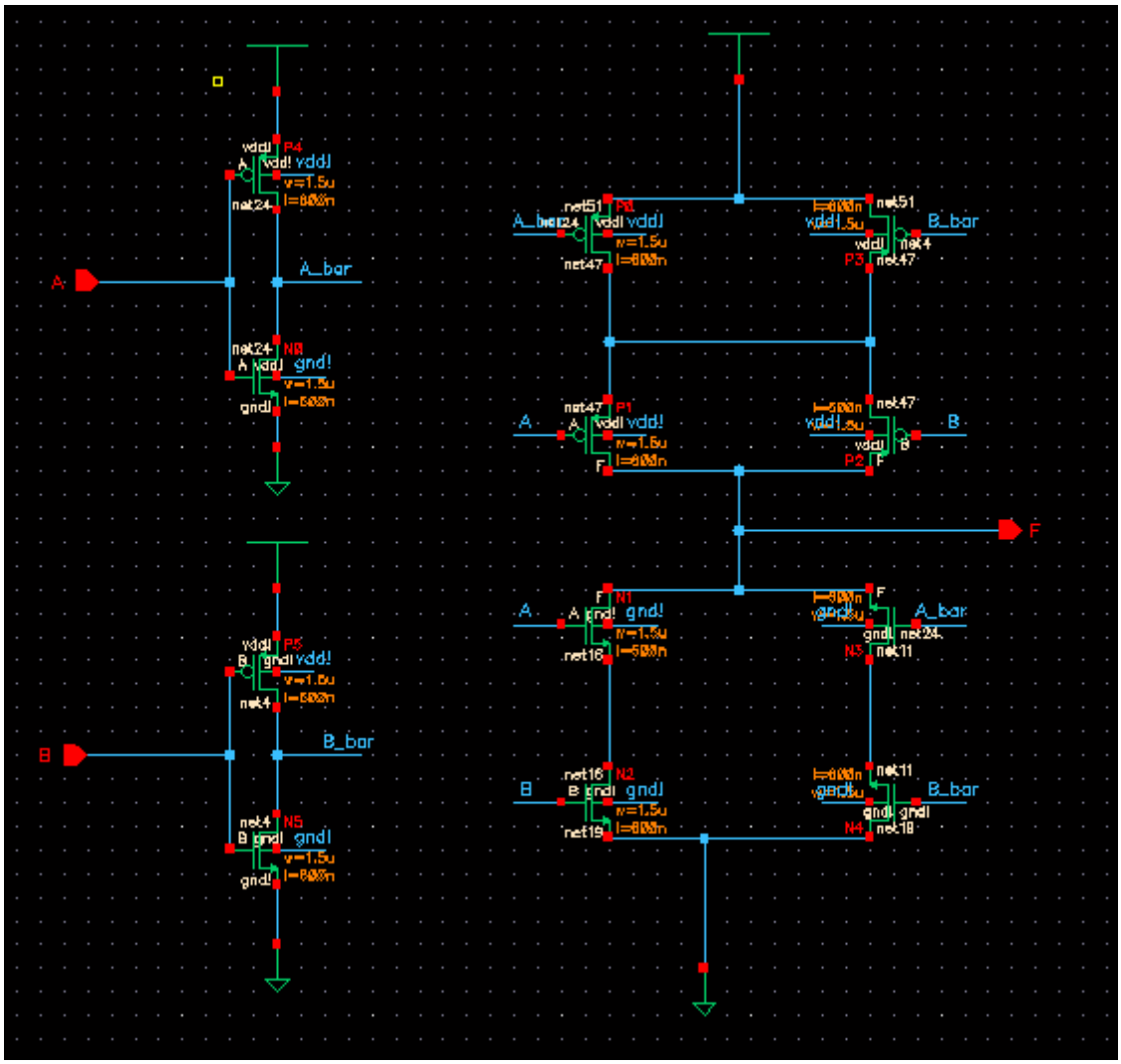
Tip #3: Using multiple vdd and gnd supply net symbols

The supply net symbols serve two primary purposes: (1) they give a visual indication of a connection to vdd or ground; and (2) they provide the global net name (vdd! or gnd!) to any wire they are connected to. You may wish to use a pair of supply symbols for each stage/gate in your schematic in order to reduce the wiring otherwise required by having only a single pair for the entire schematic. In the figure below, it is now much easier to see that the XOR schematic consists of three separate CMOS gates.



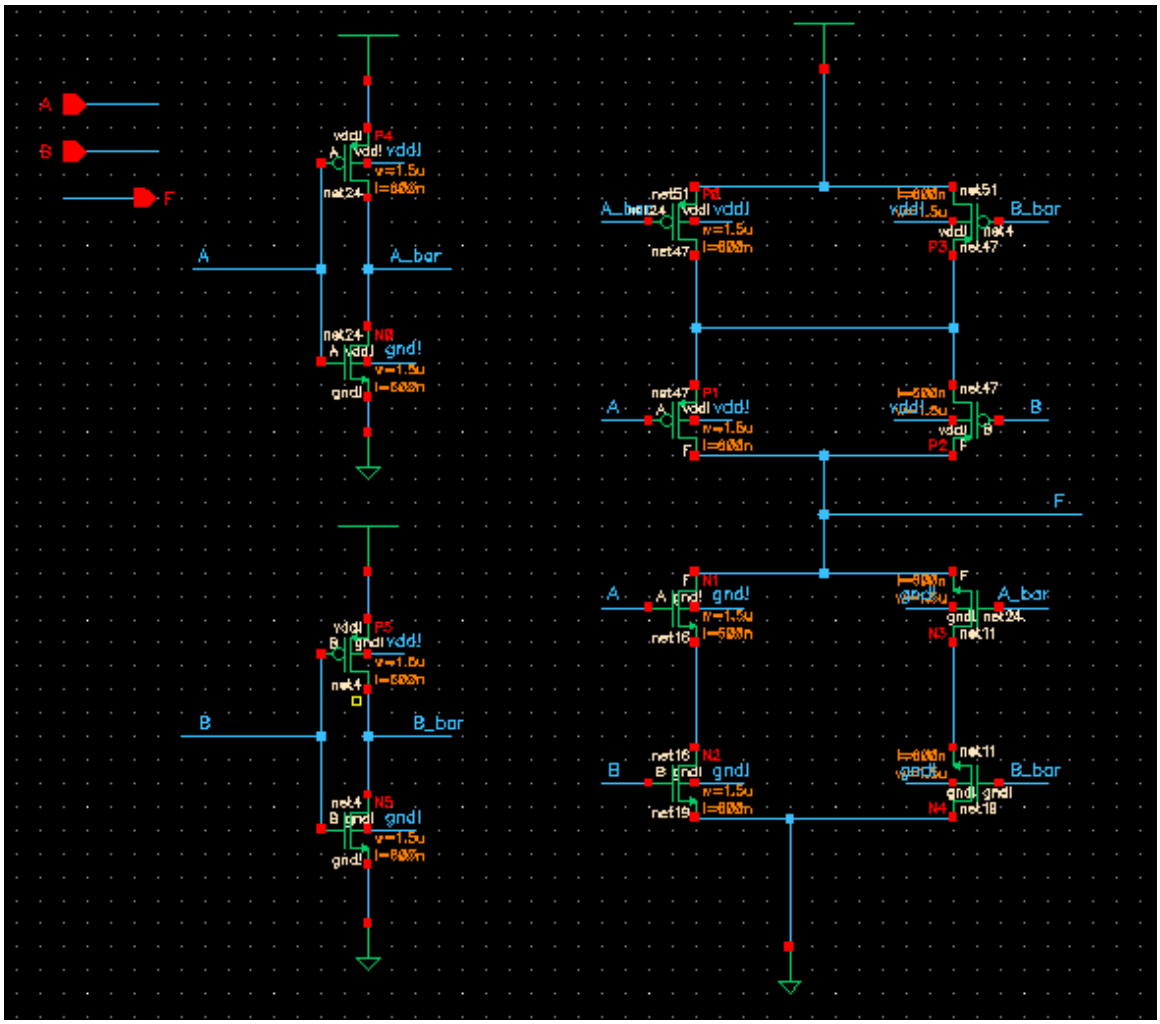
Tip #4: Give bulk connections global supply net names

Since explicit supply net connects are required for each transistor in your schematic, you can reduce a lot of wiring by connecting short wires to each transistor bulk terminal and giving it the name of the appropriate supply connection. Since labeling each transistor in this manner can be repetitive and time consuming, and may not improve the readability of the schematic very much, this use of this technique may be a matter of preference.



Tip #5: Separate pin placement from drawn circuit

For large circuits, it may be hard to find the input and output pins among a large number of transistors, wires, and supply nets. One way you might make it easier for others to identify the primary inputs and outputs it to separate them from the drawn circuit and place them to the side, as shown below. For smaller circuits, it makes less sense to do this since it does not significantly increase the readability of the schematic.



Final Note

All of the tips presented are general techniques that you can use to produce a more organized circuit schematic. While they can be very useful tools, they can also easily make schematics HARDER to read if they are used misused or abused. For instance, over-using net naming in lieu of using wire connections can it difficult to identify the type of circuit that is being modeled, and placing too many supply symbols can make the schematic difficult to decipher. You must decide when and how these techniques are best employed.
IMPORTANT: Please do not over use these methods to the point it becomes impossible to look at your schematic and see it its functionality. Some wires need to be kept!