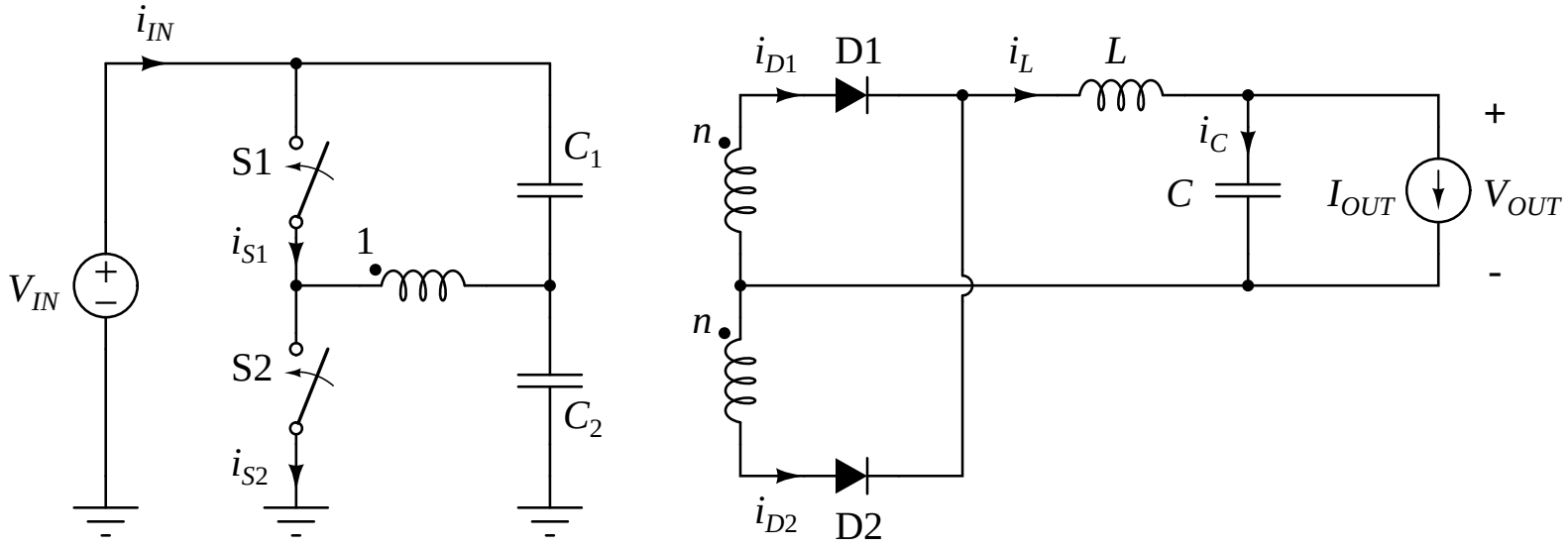
i_{IN}
S1
i_{S1}
1
V_{IN}
S2
i_{S2}
C_1
C_2
i_{D1}
D1
i_L
L
n
n
i_C
C
I_{OUT}
V_{OUT}
+
-
i_{D2}
D2