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Pulse Width Modulation in Current Source Inverters: an Algebraic Approach

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***Abstract*—This paper addresses the low-frequency part of the modulation process in current source inverters, providing the duty ratio values for the switches. The derivation is performed using purely algebraic techniques without any use of space vectors. The technique is general and applies to arbitrary waveforms of the generated current average values. Current source inverters with an arbitrary number of phases are considered. In the case of generating symmetrical polyphase currents, the maximal amplitude is derived as a function of the number of phases n. It is shown that the choice of the duty ratio values has $n-1$ degrees of freedom but within a determined range. The degrees of freedom might be used to optimize the system's performance. A simple modulator that implements the proposed technique is presented. The proposed technique is verified both by simulation and experiments.**

***Index Terms*—Current control, current supplies, pulse width modulation, pulse width modulation inverters, space vector pulse width.**

I. Introduction

This paper covers the topic of pulse width modulation in current source inverters with arbitrary number of phases. In spectral domain, results of the modulation process could be divided in the low-frequency part, below the switching frequency $f_s = 1/T_s$, and the high-frequency part, above the switching frequency. Below the switching frequency the averaging method could be applied, averaging out the high-frequency effects. This part of the spectrum is responsible for the most of the energy transfer, and average values of generated currents are shaped to meet the load requirements. The high-frequency part of the spectrum is a necessary and an unwanted follower. In the energy transfer, it contributes only to losses, and in a minor part to electromagnetic interference.

This paper addresses low-frequency part of the modulation process, aiming to develop duty ratio values for the switches to meet the load requirements. The first part of the analysis covers arbitrary values of generated current average values and derives a feasibility constraint. Next, periodic waveforms of polyphase currents are analyzed to introduce maximal amplitude and waveform scaling by a modulation index. Finally, the method is generalized to arbitrary periodic waveforms.

Nowadays, common approach to these problems relays upon space vector representation, introduced in [1]. Down to implementation, any kind of modulation reduces to a switch being turned on for some interval of time during the switching period, while being off for the remaining part. This is a pulse width modulation, and in [2] it is shown that in voltage source inverters space vector modulation reduces to common pulse width modulation where zero sequence components are added to the modulation signals.

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General form of current source inverters, discussed in this paper, is not dual to voltage source inverters [3], [4], thus the methods and conclusions could not be directly mapped from voltage source inverters. However, space vector approach migrated to the analysis of current source inverters as early as in [5], evolving from early pulse width modulation strategies [6]. It has been used since, evolving up to rather complex three dimensional space vector visualizations like [7], [8], [9]. Most of the publications that analyze current source inverters use space vectors to generate the modulation patterns, like [10], [11], [12], as summarized in [13].

Of special interest in this paper are multiphase systems, like [7], [8], [9], [14], [15], reviewed in detail in a recent publication [16]. A goal of this paper is to derive a modulation method for current source inverters that could be generalized to arbitrary number of phases.

As indicated in [2], the only information needed is whether a switch is on or off. This information is provided for all of the converter switches as the output of the modulation process. All space vector visualizations or the zero-sequence components of [2] are just human interpretations that help in the process of generating the modulation algorithm.

In this paper, low-frequency part of the modulation process is addressed such that duty ratio values of the switches are derived using algebraic techniques, without any use of space vector representation. The approach is simple and results in duty ratio values, as well as a range of freedom in their choice that might be used to optimize the system performance. Generating arbitrary average values of output currents is addressed first, and a feasibility constraint is developed. The analysis proceeds to periodic waveforms, introducing notions of amplitude, maximal amplitude and modulation index, both for symmetrical polyphase systems and arbitrary periodic waveforms. Finally, a simple modulator that implements the proposed technique is proposed, and the results are verified by simulation and experiments.

A. The Inverter

Circuit diagram of the inverter analyzed in this paper is shown in Fig. 1. The inverter consists of n phase legs, where it is assumed that $n \geq 2$. The first and the last inverter leg are presented in the circuit diagram in Fig. 1. The inverter is supplied by a DC-link current source I_{dc} and in the analysis that follows this current is assumed to be constant. The inverter consists of $2\,n$ unidirectional switches, grouped as upper switches S_{u1} to S_{un} and lower switches S_{l1} to S_{ln}.

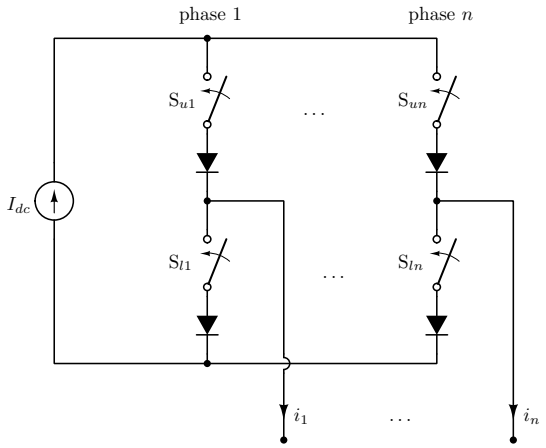


Fig. 1. The current source inverter.

Primary goal of the paper is to determine the duty ratio values d_{uk} and d_{lk} for $k \in \{1, \dots n\}$ that operate corresponding switches S_{uk} and S_{lk} to provide required average values of the inverter output currents.

Essential constraint in operating the switches is that only one switch from the upper switches group, S_{uk}, conducts at any time instant, as well as one of the switches in the lower switches group, S_{lk}. At least one switch per group is needed to provide the DC-link current flow, while the number reduces to exactly one switch per group by unidirectional switches, depicted with diodes connected in series to controlled switches in the circuit diagram of Fig. 1, utilized to avoid interphase short-circuiting at the load side.

II. Requirements, Equations, and Constraints

A. Averages of the phase currents

Averages of the phase currents over a switching period T_s in the considered inverter are

$$\langle i_k \rangle = I_{dc} \left(d_{uk} - d_{lk} \right). \tag{1}$$

The goal is to program them according to required values.

B. Flow of the DC-link current, duty ratio constraints

To provide the DC-link current flow through the upper switches, at each time point exactly one of these switches should be on. This results in the duty ratio constraint for the upper switches

$$\sum_{k=1}^{n} d_{uk} = 1. \tag{2}$$

The same applies for the lower switches, resulting in

$$\sum_{k=1}^{n} d_{lk} = 1. \tag{3}$$

C. Duty ratio limitations

Duty ratio values are always required to be within the range from 0 to 1,

$$0 \leq d_{uk} \leq 1 \tag{4}$$

and

$$0 \leq d_{lk} \leq 1. \tag{5}$$

As a consequence of the lower limit in (4) and (5) $(0 \leq)$, as well as the constraints (2) and (3), all of the upper limits of (4) and (5) (≤ 1) are implicitly satisfied, and the lower limits should be the ones taken care of.

D. Sum of the phase currents

Since the load is assumed to be connected to n output phases of the inverter only, Kirchhoff's current law implies that sum of the phase currents equals zero

$$\sum_{k=1}^{n} i_k = 0. \tag{6}$$

Averaging the above equation over the switching period, the same is derived for the averages of the phase currents

$$\sum_{k=1}^{n} \langle i_k \rangle = 0. \tag{7}$$

Substituting (1) in (7), and applying the DC-link flow constraints (2) and (3), we obtain

$$\begin{aligned} \sum_{k=1}^{n} I_{dc} \left(d_{uk} - d_{lk} \right) &= I_{dc} \left(\sum_{k=1}^{n} d_{uk} - \sum_{k=1}^{n} d_{lk} \right) \\ &= I_{dc} \left(1 - 1 \right) = 0 \end{aligned} \tag{8}$$

meaning that the sum of the phase currents constraint is implicitly satisfied by the DC-link current flow constraints. However, the form of (7) is convenient and it will be used in subsequent derivations.

E. Excess duty ratio, an important property, and minimal realization

For an inverter leg duty ratio values d_{u0k} and d_{l0k} increase in both of the duty ratio values for Δd_k results in

$$\begin{aligned} \langle i_k \rangle &= I_{dc} \left(d_{u0k} - d_{l0k} \right) \\ &= I_{dc} \left((d_{u0k} + \Delta d_k) - (d_{l0k} + \Delta d_k) \right) \end{aligned} \tag{9}$$

meaning that the average phase current remains the same. Not to affect the lower duty ratio limit for d_{u0k} and d_{l0k}, let us assume that

$$\Delta d_k \geq 0. \tag{10}$$

For $d_{u0k} + \Delta d_k$ and $d_{l0k} + \Delta d_k$ to be new duty ratio values, they should satisfy

$$0 \leq d_{u0k} + \Delta d_k \leq 1 \tag{11}$$

and

$$0 \leq d_{l0k} + \Delta d_k \leq 1 \tag{12}$$

where the lower limit is implicitly satisfied by (10) as d_{u0k} and d_{l0k} are already the duty ratio functions, and the upper limit remains to be satisfied.

Minimal realization is defined by d_{u0k} and d_{l0k} values which satisfy that either $d_{u0k} = 0$ either $d_{l0k} = 0$ during a considered switching period. In the case of nonminimal

realization, $d_{uk} > 0$ and $d_{lk} > 0$, and corresponding minimal realization is obtained by

$$d_{u0k} = d_{uk} - \min\left(d_{uk},\, d_{lk}\right) \tag{13}$$

and

$$d_{l0k} = d_{lk} - \min\left(d_{uk},\, d_{lk}\right) \tag{14}$$

as the excess duty ratio at phase k is then given by

$$\Delta d_k = \min\left(d_{uk},\, d_{lk}\right). \tag{15}$$

F. Summary of the problem

Our goal in this paper is to determine the duty ratio values d_{uk} and d_{lk} that provide required values of averaged phase currents $\langle i_k \rangle$ and satisfy constraints (2), (3), (4), and (5). The problem reduces to a linear algebra problem of a set of linear equations that can be summarized as follows:

1) There are 2 n unknown variables, d_{uk} and d_{lk} for $k \in \{1, \dots n\}$.
2) There are two constraints, imposed by the requirement of the DC-link current flow, $\sum_{k=1}^{n} d_{uk} = 1$ and $\sum_{k=1}^{n} d_{lk} = 1$, both of which are linear equations.
3) There are n equations that specify $\langle i_k \rangle$, as determined by (1), all of them are linear equations over d_{uk} and d_{lk}.
4) One equation from the previous group of equations over $\langle i_k \rangle$ is redundant since $\sum_{k=1}^{n} \langle i_k \rangle = 0$.

Counting the equations and the unknown variables, we can conclude that the system of equations does not have a unique solution, since there are

$$n_{df} = 2\,n - 2 - (n-1) = n - 1 \tag{16}$$

degrees of freedom, i.e. variables that can be chosen arbitrarily, but within a certain range to satisfy (4) and (5).

III. Obtaining the Duty Ratio Values

Let us consider a set of average values of a current source inverter output currents $\langle i_k \rangle$ for $k \in \{1, \dots n\}$ that satisfies constraint (7) that are required to obtain from a DC source I_{dc} where it is assumed $I_{dc} > 0$. Using the Heaviside step function

$$\mathrm{h}\left(x\right) = \begin{cases} 0 & x < 0 \\ \frac{1}{2} & x = 0 \\ 1 & x > 0. \end{cases} \tag{17}$$

to provide compact notation, these average currents could be decomposed in their positive and negative parts

$$\langle i_k \rangle_+ = \langle i_k \rangle\, \mathrm{h}\left(\langle i_k \rangle\right) \tag{18}$$

and

$$\langle i_k \rangle_- = -\langle i_k \rangle\, \mathrm{h}\left(-\langle i_k \rangle\right) \tag{19}$$

resulting in

$$\langle i_k \rangle = \langle i_k \rangle_+ - \langle i_k \rangle_- \tag{20}$$

where both of the values (18) and (19) are nonnegative.

In practice, application of the Heaviside function is not computationally efficient, and it is used here just to provide compact notation. Instead, two distinct branching based functions would be used to separate positive and negative parts.

According to (1) and the notions introduced in Section II-E, minimal realizations of the duty ratio values are

$$d_{u0k} = \frac{\langle i_k \rangle_+}{I_{dc}} \tag{21}$$

and

$$d_{l0k} = \frac{\langle i_k \rangle_-}{I_{dc}} \tag{22}$$

where at least one of them equals zero. It should be noted that according to (7), (20), (21), and (22)

$$\sum_{k=1}^{n} d_{u0k} = \sum_{k=1}^{n} d_{l0k}. \tag{23}$$

Feasibility constraint for the given problem is

$$\sum_{k=1}^{n} d_{u0k} \leq 1 \tag{24}$$

and the inequality applies in the same form to d_{l0k} according to (23), making it redundant. To satisfy constraints for the flow of the DC-link current (2) and (3), total excess duty ratio is defined as

$$\Delta d = 1 - \sum_{k=0}^{n} d_{u0k} \tag{25}$$

and in the case the required current average values $\langle i_k \rangle$ are feasible for a given value of I_{dc}, it has a nonnegative value

$$\Delta d \geq 0. \tag{26}$$

To satisfy (2) and (3) the excess duty ratio values Δd_k should satisfy

$$\sum_{k=1}^{n} \Delta d_k = \Delta d. \tag{27}$$

To fulfill this requirement, there are n unknown variables, Δd_k, and one constraint (27), which corresponds in $n-1$ degrees of freedom (16) to chose Δd_k values. These degrees of freedom may be used to perform optimization. One solution for a given problem is to share Δd to Δd_k values equally

$$\Delta d_k = \frac{1}{n}\,\Delta d \tag{28}$$

which may be used just to provide actual d_{uk} and d_{lk} values without any optimization, resulting in

$$d_{uk} = d_{u0k} + \frac{1}{n}\,\Delta d \tag{29}$$

and

$$d_{lk} = d_{l0k} + \frac{1}{n}\,\Delta d \tag{30}$$

where d_{u0k}, d_{l0k} and Δd are defined by (21), (22), and (25).

In this manner, the current source inverter modulation process is resolved in general case without any use of space vectors.

IV. The Case of Sinusoidal Symmetrical Polyphase Currents

A case of special interest in practice is the case of symmetrical polyphase currents with the average values

$$\langle i_k \rangle (\omega_0 t) = I_m \cos\left(\omega_0 t - (k-1)\,\frac{2\,\pi}{n}\right) \tag{31}$$

for for $k \in \{1, \dots n\}$. It should be noted that $\langle i_k \rangle = \langle i_k \rangle (\omega_0 t)$ is a function of time t, or equivalently of the phase angle $\omega_0 t$, which introduces notions such as the waveform period T_0, frequency $f_0 = 1/T_0$, angular frequency $\omega_0 = 2\,\pi\,f_0$, and amplitude I_m. In comparison to the general case analyzed in Section III, where generated currents are analyzed within the scope of one switching period, in this case the scope is expanded to one line cycle period, i.e. the waveform period. Further development of this analysis would yield a maximal amplitude that can be achieved and a modulation index that scales down the achievable waveforms.

According to (1),

$$I_{dc}\,(d_{uk} - d_{lk}) = I_m \cos\left(\omega_0 t - (k-1)\,\frac{2\,\pi}{n}\right) \tag{32}$$

and we aim the duty ratio functions d_{uk} and d_{lk} over a line period as functions of $\omega_0 t$. In this aim, three questions arise:

1) How big $I_{m\,max} = \max(I_m)$ that can be realized under constraints (4) and (5) is?
2) How the duty ratio functions d_{uk} and d_{lk} depend on the phase current amplitude I_m for $0 \le I_m \le I_{m\,max}$?
3) How the value of Δd depends on the phase current amplitude I_m for $0 \le I_m \le I_{m\,max}$?

A. Minimal realizations of the phase currents

First, let us determine the minimal realizations. For the notational convenience, let us define the phase angle variable for the k^{th} phase as

$$\varphi_k (\omega_0 t) = \omega_0 t - (k-1)\,\frac{2\,\pi}{n} \tag{33}$$

resulting in

$$\langle i_k \rangle (\omega_0 t) = I_m \cos(\varphi_k (\omega_0 t)). \tag{34}$$

Next, let us define two auxiliary functions

$$u_k (\omega_0 t) = \cos(\varphi_k (\omega_0 t))\ \mathrm{h}(\cos(\varphi_k (\omega_0 t))) \tag{35}$$

and

$$l_k (\omega_0 t) = -\cos(\varphi_k (\omega_0 t))\ \mathrm{h}(-\cos(\varphi_k (\omega_0 t))) \tag{36}$$

in the manner of (18) and (19), again as a notational convenience. Functions $u_k (\omega_0 t)$ and $l_k (\omega_0 t)$ satisfy

$$0 \le u_k (\omega_0 t) \le 1 \tag{37}$$

and

$$0 \le l_k (\omega_0 t) \le 1 \tag{38}$$

the same constraints as imposed to duty ratio values. It should also be noted that

$$\cos(\varphi_k (\omega_0 t)) = u_k (\omega_0 t) - l_k (\omega_0 t) \tag{39}$$

which is decomposition of the cosine function to minimal positive values.

Maximum of the phase current average value amplitude that can be obtained applying the analyzed current source inverter is according to (1) linearly dependent on the DC-link current

$$I_{m\,max} = a\,I_{dc} \tag{40}$$

where a is the amplitude parameter, dependent on the number of phases n.

From (1), (39), and (40), the minimal realization is

$$I_{dc}\,(d_{u0k} (\omega_0 t) - d_{l0k} (\omega_0 t)) = a\,I_{dc}\,(u_k (\omega_0 t) - l_k (\omega_0 t)) \tag{41}$$

which is satisfied for

$$d_{u0k} (\omega_0 t) = a\,u_k (\omega_0 t) \tag{42}$$

and

$$d_{l0k} (\omega_0 t) = a\,l_k (\omega_0 t). \tag{43}$$

According to (7), (31), and (39), we have

$$\sum_{k=1}^{n} \cos(\varphi_k (\omega_0 t)) = \sum_{k=1}^{n} u_k (\omega_0 t) - \sum_{k=1}^{n} l_k (\omega_0 t) = 0 \tag{44}$$

resulting in

$$\sum_{k=1}^{n} u_k (\omega_0 t) = \sum_{k=1}^{n} l_k (\omega_0 t) \tag{45}$$

which is an important property to be used in the subsequent derivation.

B. Maximum of the phase current amplitude

Maximum of the phase current amplitude that can be obtained by the analyzed inverter is limited by the duty ratio constraints (2) and (3). It should be noted here that $\sum_{k=1}^{n} u_k = \sum_{k=1}^{n} l_k$ are not constant, thus neither are $\sum_{k=1}^{n} d_{u0k}$ and $\sum_{k=1}^{n} d_{l0k}$, regardless the fact that with increasing of the number of phases n these values are getting closer to a constant value. Since d_{u0k} and d_{l0k} correspond to minimal realization, corresponding actual duty ratio values

$$d_{uk} (\omega_0 t) = d_{u0k} (\omega_0 t) + \Delta d_k (\omega_0 t) \tag{46}$$

and

$$d_{lk} (\omega_0 t) = d_{l0k} (\omega_0 t) + \Delta d_k (\omega_0 t) \tag{47}$$

should be increased over the minimal realization for Δd_k to make the sums equal to one. Since $\Delta d_k \ge 0$, the minimal realization duty ratio values should satisfy

$$\sum_{k=1}^{n} d_{u0k} (\omega_0 t) \le 1 \tag{48}$$

and

$$\sum_{k=1}^{n} d_{l0k} (\omega_0 t) \le 1 \tag{49}$$

which is the same constraint as a consequence of (42), (43), and (45). So, let us focus to (48) as sufficient, which results in

$$a \sum_{k=1}^{n} u_k (\omega_0 t) \le 1. \tag{50}$$

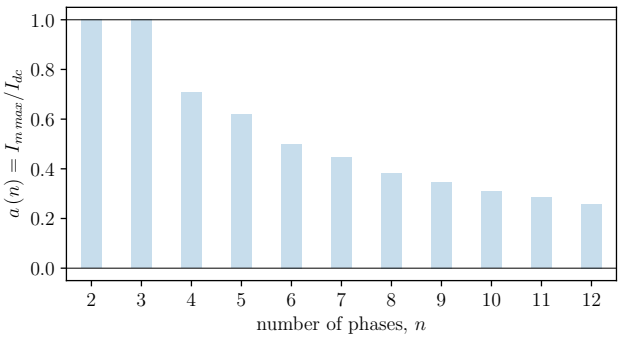


Fig. 2. Maximum amplitude parameter as it depends on the number of phases, $a(n)$.

At this point, it is convenient to define an auxiliary function $w(\omega_0 t)$ as

$$w(\omega_0 t) = \sum_{k=1}^{n} u_k(\omega_0 t). \tag{51}$$

This leads to the definition of w_{max} as

$$w_{max} = \max_{0 \le \omega_0 t \le 2\pi} w(\omega_0 t) \tag{52}$$

and from the maximum amplitude constraint (50)

$$a\, w_{max} = 1 \tag{53}$$

we finally obtain

$$a = \frac{1}{w_{max}} \tag{54}$$

which according to (40) determines maximum of the phase current amplitude. This also limits the minimal realization duty ratio functions to $d_{u0k} \le a$ and $d_{l0k} \le a$.

The value of a depends on the number of phases n, making it a function of the inverter number of phases, $a(n)$. Numerically computed values of $a(n)$ for $2 \le n \le 12$ are given in Fig. 2. For the single-phase inverter, $n = 2$, as well as for the three-phase inverter, $n = 3$, maximal amplitude of the phase currents equals to the DC-link current. However, for higher number of phases the maximal amplitude is lower than the DC-link current according to the $a(n)$ function that asymptotically approaches $I_m = \frac{\pi}{n} I_{dc}$ as $n \to \infty$, since I_{dc} approaches a sum of the output current of n half-wave rectifiers interleaved such that ripple of the sum over a line period is getting negligible.

C. Variable amplitude of the phase currents

After the minimal realization of the duty ratio functions is determined, as well as the maximum of the phase currents, the next task is to determine minimal realizations of the duty ratio functions for arbitrary amplitude of the phase currents

$$I_m = m\, I_{m\,max} = m\, a\, I_{dc} \tag{55}$$

where m is the modulation index

$$0 \le m \le 1 \tag{56}$$

which scales down the waveforms. Since

$$\begin{aligned} \langle i_k \rangle(\omega_0 t) &= m\, I_{m\,max}\, \cos(\varphi_k(\omega_0 t)) \\ &= m\, a\, I_{dc}(u_k(\omega_0 t) - l_k(\omega_0 t)) \end{aligned} \tag{57}$$

the minimal realization duty ratios in the case of the arbitrary amplitude are

$$d_{u0k}(\omega_0 t) = m\, a\, u_k(\omega_0 t) \tag{58}$$

and

$$d_{l0k}(\omega_0 t) = m\, a\, l_k(\omega_0 t). \tag{59}$$

It should also be noted here that according to (23) sum of the upper duty ratio functions equals the sum of the lower duty ratio functions, which are functions of the phase angle now

$$\sum_{k=1}^{n} d_{u0k}(\omega_0 t) = \sum_{k=1}^{n} d_{l0k}(\omega_0 t). \tag{60}$$

In minimal realizations, these sums are not constant, neither always equal to one.

D. Excess of the duty ratio

To satisfy the requirements of (2) and (3), duty ratio values d_{uk} and d_{lk} should be increased over their minimal realization values d_{u0k} and d_{l0k} for Δd_k according to (9). The total extra duty ratio (25) Δd now becomes a function of the phase angle

$$\Delta d(\omega_0 t) = \sum_{k=1}^{n} \Delta d_k(\omega_0 t) \tag{61}$$

the same as particular duty ratio excess values Δd_k. According to (25)

$$\Delta d(\omega_0 t) = 1 - \sum_{k=1}^{n} d_{u0k}(\omega_0 t) \tag{62}$$

and it should be distributed into n possibly different Δd_k values, which brings $n-1$ degree of freedom in our problem of obtaining the duty ratio values, again.

Since according to (51)

$$\sum_{k=1}^{n} d_{u0k}(\omega_0 t) = m\, a \sum_{k=1}^{n} u_k(\omega_0 t) = m\, a\, w(\omega_0 t) \tag{63}$$

the total excess duty ratio is obtained as

$$\Delta d(\omega_0 t) = 1 - m\, a\, w(\omega_0 t) \tag{64}$$

and depends on the modulation index. Again, one solution is to spread Δd over Δd_k equally (28)

$$\Delta d_k(\omega_0 t) = \frac{1}{n} \Delta d(\omega_0 t) = \frac{1}{n} (1 - m\, a\, w(\omega_0 t)). \tag{65}$$

This analysis is just an application of the method described in Section III to the case of symmetrical polyphase currents, which introduces notions of the maximum amplitude parameter a and the modulation index m by observing the waveforms on the line period level, that is wider than the switching period level used in Section III.

E. Examples

To illustrate the modulation technique, in the left column of Fig. 3 waveforms of the minimal realization duty ratios d_{u01} and d_{l01} are presented, as well as the total excess duty ratio function Δd for the inverters ranging from $n = 2$ (which is a single phase inverter) to $n = 5$ phases, with the modulation index $m = 1$ corresponding to the maximal amplitude, while in the right column of Fig. 3 the same values are presented for $m = 0.5$, that corresponds to one half of the maximal amplitude. The duty ratio values d_{u0k} and d_{l0k} for phases other than $k = 1$ are just phase shifted right for $(k-1)\,\frac{2\pi}{n}$.

Analyzing the diagrams of Fig. 3, as well as the diagrams that correspond to higher number of phases not presented here, it is concluded that Δd variation is higher for even values of n in comparison to the surrounding odd phase number values $n-1$ and $n+1$. Also, the waveform of Δd is periodic with T_0/n for even number of phases n, where T_0 is the line period, while it is periodic with $T_0/(2\,n)$ for odd number of phases, doubling the frequency. Furthermore, the span covered by the excess duty ratio Δd is higher for lower modulation index values, as predicted by (64), reaching its maximum for $m = 0$. Increasing the number of phases reduces variation in Δd over the line period.

To illustrate actual duty ratio values, waveforms of d_{u1} and d_{l1} are presented in the left column of Fig. 4, for the modulation index $m = 1$, corresponding to the maximal amplitude, and for the number of phases varying from $n = 2$ to $n = 5$, again. The line corresponds to equal sharing of the total excess duty ratio according to (65), while the shaded area represents values that can be reached by different algorithms of sharing the excess duty ratio. Corresponding diagrams for the modulation index of $m = 0.5$ are presented in the right column of Fig. 4, indicating lower duty ratio values and wider span of achievable duty ratio values.

V. Generalization to Arbitrary Periodic Waveforms

The analysis of periodic waveforms of generated currents presented up to this point covers symmetrical sinusoidal polyphase currents. To preserve notions of amplitude I_m, maximal amplitude parameter a, and the modulation index m, the method could easily be generalized to arbitrary periodic waveforms of the output current averaged values that satisfy constraint (7). This generalization might be of interest to cover unbalanced sinusoidal waveforms [7], [8], [9], [15], overmodulation, and any other periodic waveforms of generated currents.

The first step in this generalization is to generalize the notion of amplitude I_m, and it is defined here as a maximum absolute value of output current average values as

$$I_m = \max_{1\le k\le n}\left(\max_{0\le t\le T_0}\left(\left|\,\langle i_k\rangle\,(t)\,\right|\right)\right). \tag{66}$$

This choice affects the definitions of auxiliary functions (35) and (36), redefining them as

$$u_k = \frac{\langle i_k\rangle}{I_m}\;\mathrm{h}\left(\frac{\langle i_k\rangle}{I_m}\right) \tag{67}$$

and

$$l_k = -\frac{\langle i_k\rangle}{I_m}\;\mathrm{h}\left(-\frac{\langle i_k\rangle}{I_m}\right) \tag{68}$$

which reduces to (35) and (36) in the symmetrical polyphase sinusoidal case. This choice of I_m provides that values of u_k and l_k satisfy (37) and (38), making it possible for $I_{dc} \ge I_m$ to realize each of $\langle i_k\rangle$ values according to (1) as a single current, regardless of other currents.

After the definitions of u_k and l_k are generalized, the analysis proceeds in the same way, with the same definitions of w (51), w_{max} (52), and a (54), resulting in the value of a that makes realization of all $\langle i_k\rangle$ values for $k \in \{1, \ldots n\}$ from I_{dc} feasible, modeling their interaction.

Finally, minimal realizations d_{u0k} and d_{l0k} are obtained according to (58) and (59), resulting in the total excess duty ratio Δd of (64), which is then shared to particular excess duty ratio values Δd_k.

Resulting duty ratio waveforms would be different than presented in Figs. 3 and 4, depending on the required currents, but the analysis would be the same.

In this manner, notion of the amplitude is generalized to (66), affecting notions of the maximal amplitude parameter (54) and the modulation index (55) for an arbitrary set of periodic phase current waveforms. It is worth to underline here that the amplitude I_m is chosen to be able to generate each of the $\langle i_k\rangle$ currents out of I_{dc} solely, regardless of other currents. Amplitude parameter a is introduced to model mutual effects of generated currents, and to make it feasible to generate the set of all phase currents out of I_{dc}, which sometimes requires scaling down them by $a < 1$. Finally, modulation index m is introduced to scale down feasible waveforms of $\langle i_k\rangle$ proportionally, when and if needed.

VI. The Modulator

After the duty ratio algorithm is described in Section III, a problem that follows is how to design a pulse width modulator circuit that provides computed duty ratio values and additionally provides the switching sequence such that a switch is turned off just an overlap time after the next conducting switch is turned on, in order to provide continuous flow of the DC-link current during the switch commutation. Two modulators are required, for the upper switches, and for the lower switches. In this section, a modulator design is illustrated in the case of generating control signals for the upper switches for an inverter with three phases, $n = 3$.

One solution of the modulator is based on the normalized waveforms presented in Fig. 5: the time variable is normalized to the switching period T_s, while the voltage waveforms are normalized to the sawtooth waveform generator amplitude V_m. In Fig. 5, a sawtooth waveform is compared to $n-1$ threshold levels, which is two in the three-phase case. The levels are set to d_{u1} and $d_{u1} + d_{u2}$, or in general case from d_{u1} up to $\sum_{k=1}^{n-1} d_{uk}$, and provided to the comparators shown in Fig. 6. This results in auxiliary signals s_{u1} up to $s_{u\,(n-1)}$, the last being s_{u2} in the considered $n = 3$ case. Signals s_{u1} and s_{u2} are also shown in Fig. 5. These auxiliary signals are fed to the logic circuitry of Fig. 7 which provides the switch

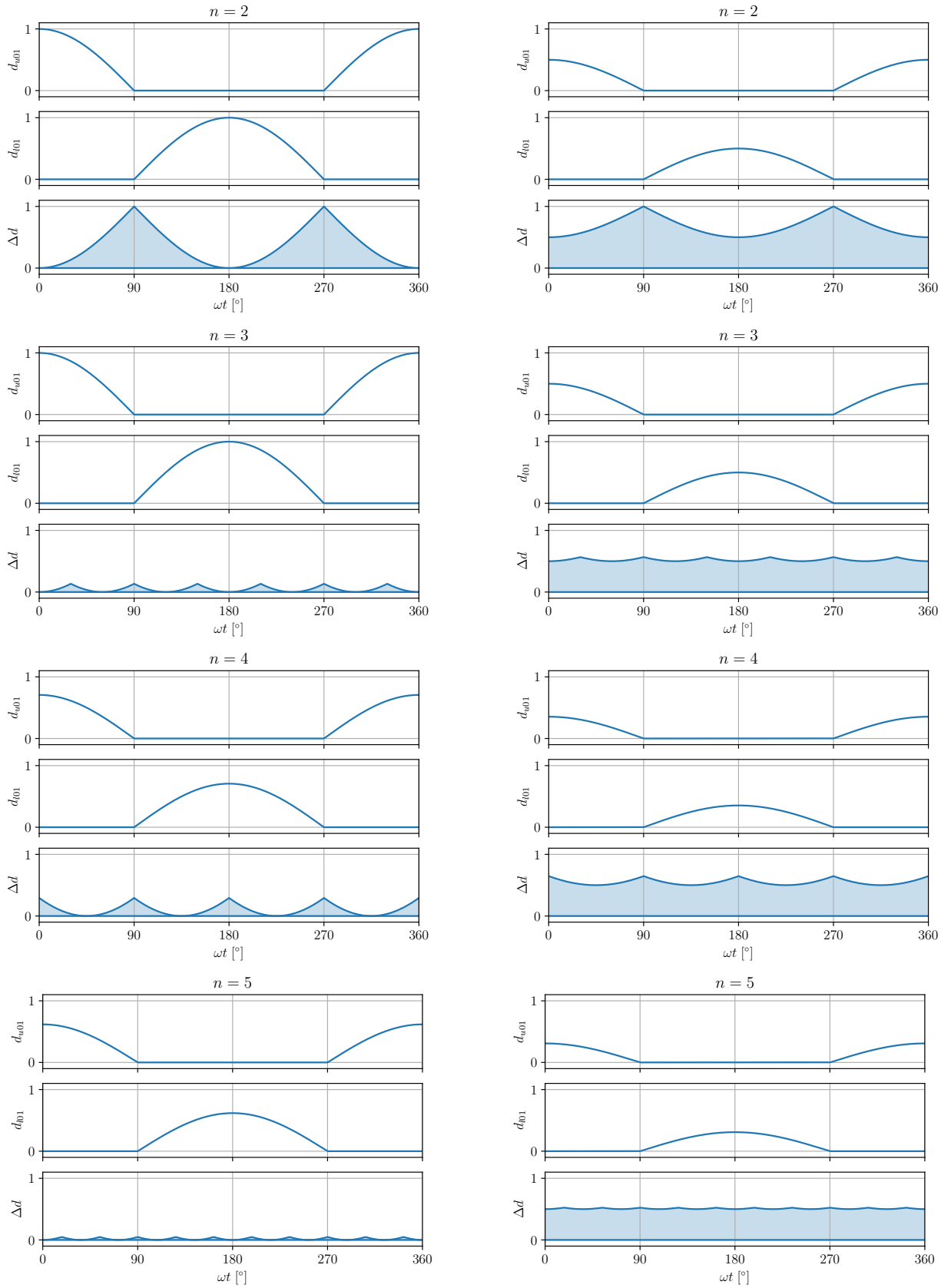


Fig. 3. Duty ratio functions d_{u01}, d_{l01}, and Δd: left column, $m = 1$; right column, $m = 0.5$.

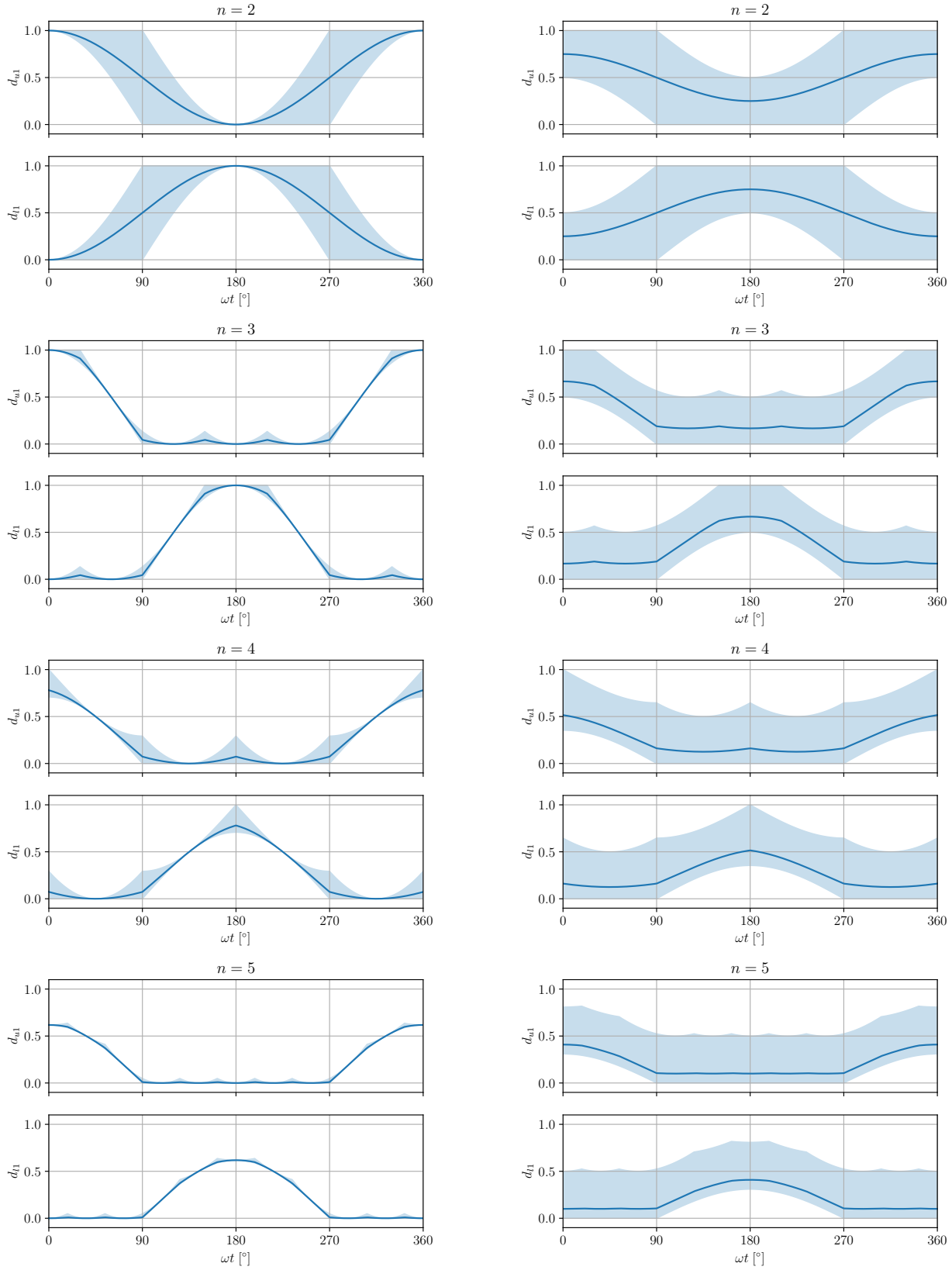


Fig. 4. Duty ratio functions d_{u1} and d_{l1}: left column, $m = 1$; right column, $m = 0.5$.

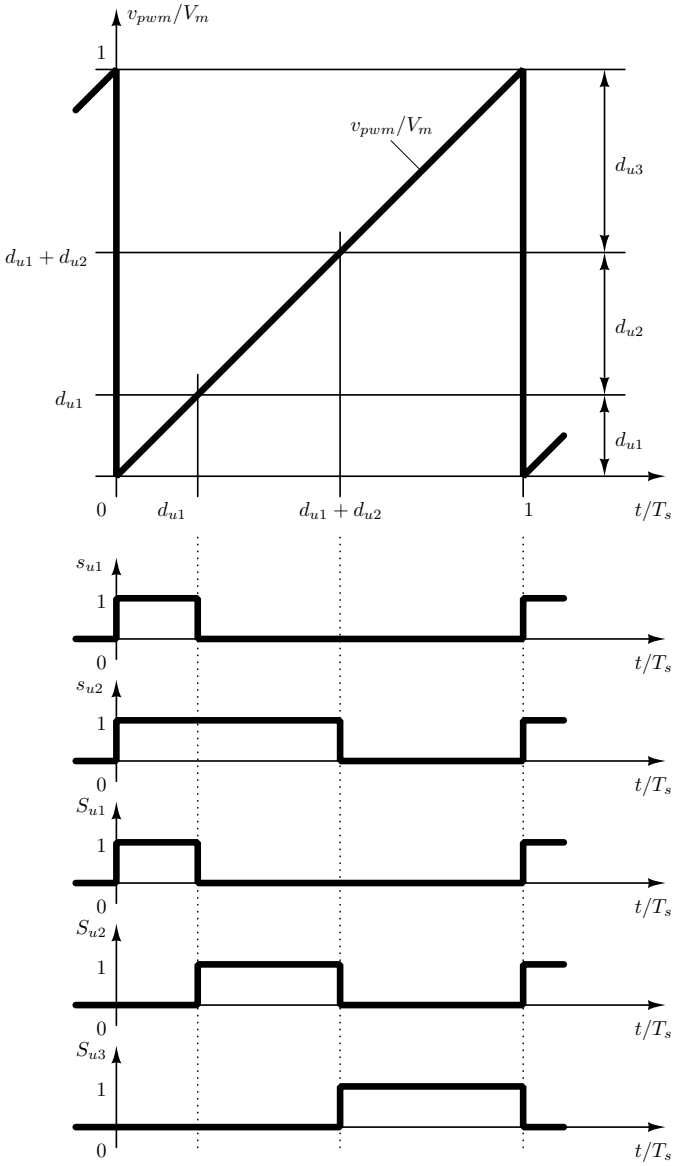


Fig. 5. Pulse width modulator waveforms.

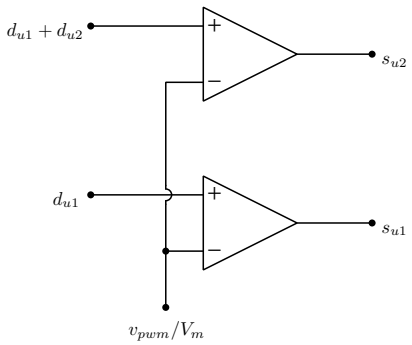


Fig. 6. Pulse width modulator comparators.

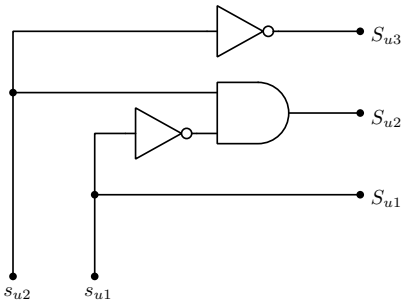


Fig. 7. Pulse width modulator logic circuitry.

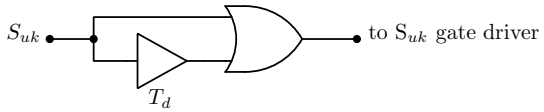


Fig. 8. Logical structure of the overlap circuit.

gating signals such that $S_{u1} = s_{u1}$, $S_{un} = \neg s_{u\,(n-1)}$, while $S_{uk} = s_{uk} \wedge \neg s_{u\,(k-1)}$ for all of the k values other than 1 and n. Finally, to provide the overlap of gating signals during commutation of the switches, an overlap circuit with a logical structure presented in Fig. 8 is used. The buffer in the circuit of Fig. 8 provides the time delay T_d, which delays falling edge of the gating signal, while the or circuit provides prompt turning on.

Proposed modulator requires one sawtooth or triangular waveform generator, $2\,n - 2$ comparators, $2\,n - 2$ logic inverters, and $2\,n - 4$ logic and circuits with two inputs, as well as $2\,n$ overlap circuits, each consisting of a delay buffer and a logical or circuit with two inputs.

A. Generalization of the modulator carrier waveform

The carrier waveform shown in Fig. 5 is assumed as a sawtooth one. However, any triangular waveform consisting of two linear segments would provide the same duty ratio values, and the shape of the waveform might be used to optimize the high-frequency part of the generated currents spectra. In that sense, instead of the waveform v_{pwm}/V_m of Fig. 5 that rises from 0 to 1 for $0 \leq t/T_s < 1$ and falls back down to zero vertically at $t/T_s = 1$, a waveform with linear rise from 0 to 1 for $0 \leq t/T_s < \alpha$ and linear fall from 1 to 0 for $\alpha \leq t/T_s < 1$ could be used. The value of α might be used as an additional optimization parameter that affects the high-frequency spectrum. A case of $\alpha = 0.5$ is used to generate experimental results presented here.

Furthermore, it is worth to mention that carrier waveforms for the upper set of duty ratio values d_{uk} and the lower set of duty ratio values d_{lk} in the proposed modulator do not have to be the same, neither mutually synchronized.

VII. Application Examples

In this section, the proposed algebra-based modulation method is used to illustrate pulse width modulation applied in current source inverters in two examples.

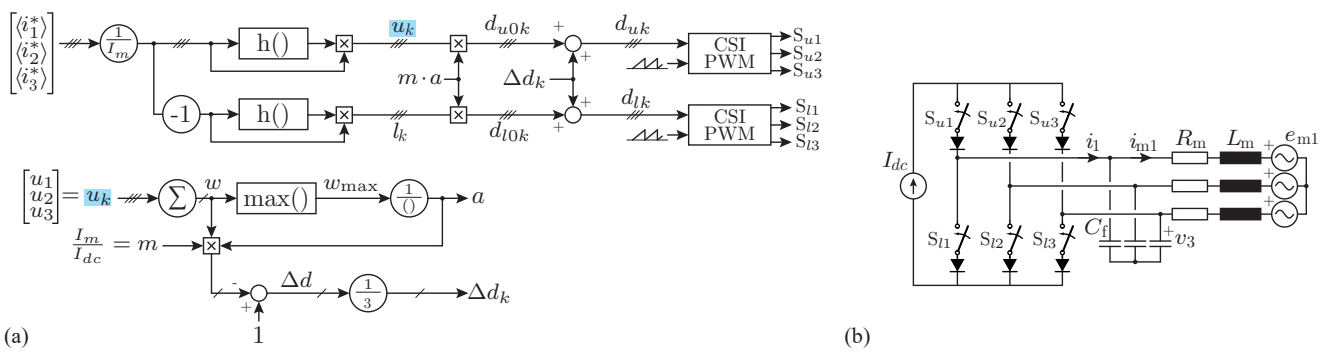


Fig. 9. (a) Block diagram of the proposed algebra-based modulation for the current source converters. (b) Three-phase inverter example supplying a three-phase permanent magnet machine.

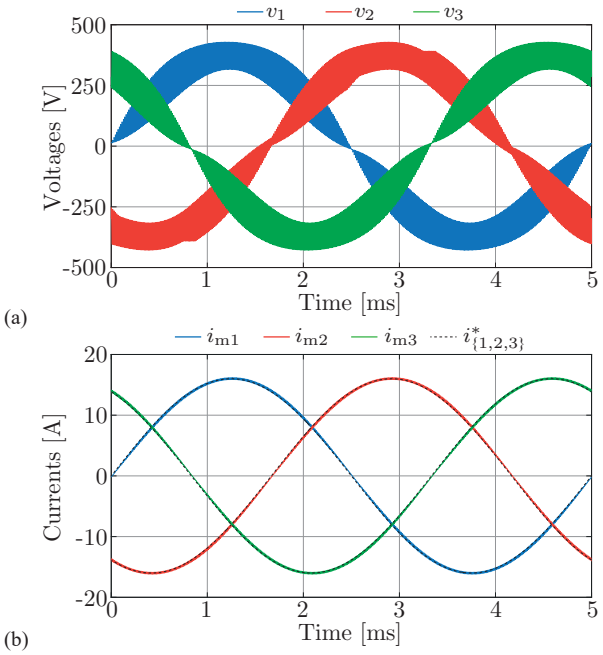


Fig. 10. (a) Voltages of the filter capacitors at the output of the inverter. (b) Current reference and the actual motor current. A slight phase shift of the current with respect to the reference can be observed due to capacitor current.

A. Symmetrical load, sinusoidal currents, three-phase

Using the derivations explained previously, the modulation technique is outlined in a block diagram in Fig. 9(a) as it has been applied in a commercial simulation tool. The inputs to the modulation process include three-phase current references (i_1^*, i_2^*, and i_3^*), alongside the modulation index m. The duty cycles obtained for the upper-side (d_{u1}, d_{u2}, d_{u3}) and lower-side (d_{l1}, d_{l2}, d_{l3}) switches are then provided to the modulator (see Figs. 6 and 7), which generates the gate driver signal commands (S_{u1}, S_{u2}, S_{u3}, S_{l1}, S_{l2}, S_{l3}) that are directly conveyed to the gate drivers of the switches illustrated in Fig. 9(b).

In the example under consideration, the modulation index is set to $m = 0.8$, where $I_{dc} = 20\,\mathrm{A}$, resulting in a peak phase current of $m\,I_{\mathrm{dc}} = 16\,\mathrm{A}$. The motor has a resistance specified as $R_{\mathrm{m}} = 3\,\Omega$, and an inductance of $L_{\mathrm{m}} = 0.6\,\mathrm{mH}$. Output power of the motor is $7.8\,\mathrm{kW}$, corresponding to a peak back EMF of $324\,\mathrm{V}$. Related waveforms are depicted in Fig. 10. To ensure the motor windings are protected, a filter capacitance of $C_f = 0.1\,\mu\mathrm{F}$ is chosen. This is to keep the dv/dt of the phase voltages v_1, v_2, and v_3 below $1\,\mathrm{V/ns}$, a value considered safe for the motor windings. With a switching frequency of $72\,\mathrm{kHz}$, the high-frequency voltage ripple is illustrated in Fig. 10(a), and the resulting motor currents are presented in Fig. 10(b).

The results underscore the simplicity and effectiveness of employing the proposed algebra-based modulation technique for current source inverters. This approach is notably more straightforward than implementing apace vector modulation for current source inverters — a method that, despite its complexity, continues to be frequently discussed and utilized in literature. Adopting our proposed methodology eradicates the necessity for employing space vector modulation in current source inverters, offering a more efficient and less complicated alternative for modulation.

B. Sinusoidal currents, the load is not symmetrical, four-phase

The next simulation example covers a four-leg current source inverter structure intended to cover imbalances in a three-phase load connected using a four-wire connection. Similar structures were analyzed in several publications [7], [8], [9], [15], some of them recent, but significantly more complex methods were used for the modulation design there. The four of the inverter phase currents are assumed as unbalanced, such that $i_1 = 10\,\mathrm{A}\cos(\omega_0 t)$, $i_2 = 9\,\mathrm{A}\cos\left(\omega_0 t - \frac{2\pi}{3}\right)$, $i_3 = 8\,\mathrm{A}\cos\left(\omega_0 t - \frac{4\pi}{3}\right)$, and $i_4 = -i_1 - i_2 - i_3$. The switching frequency is set to $f_s = 140\,\mathrm{kHz}$, while capacitors of $C_f = 5\,\mu\mathrm{F}$ were used at the load side to provide some filtering, as well as the inductors of $L_1 = L_2 = L_3 = 50\,\mu\mathrm{H}$. The DC-link current is $I_{dc} = 15\,\mathrm{A}$. The load resistors are not symmetrical, their values are $R_1 = 10\,\Omega$, $R_2 = 11.1\,\Omega$, and $R_3 = 12.5\,\Omega$, instead. The values are chosen to provide symmetrical load voltages with the amplitude equal to $V_m = 100\,\mathrm{V}$.

The converter, as well as its control system, are presented in the circuit diagram of Fig. 11. Resulting waveforms are presented in Fig. 12, being in complete agreement with the predictions, illustrating simplicity of the control method as being generalized to unbalanced loads.

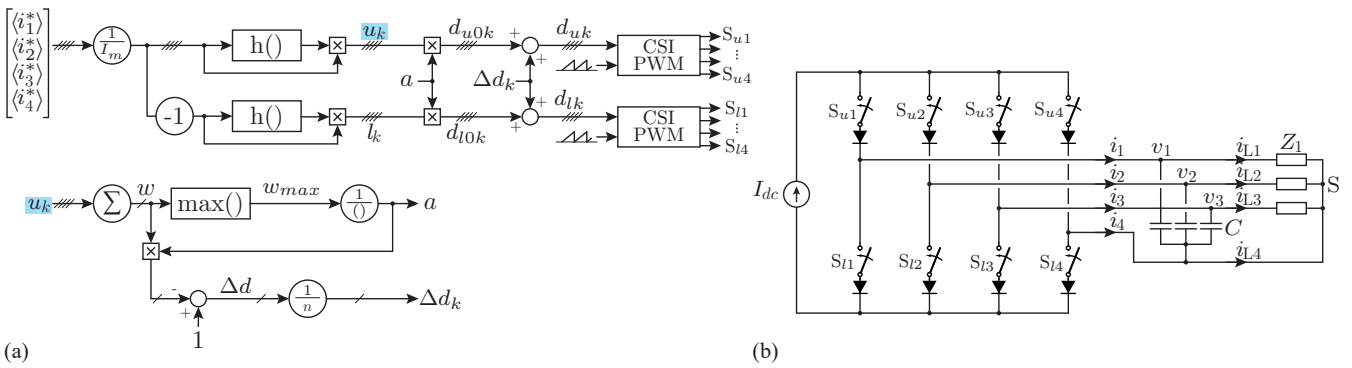


Fig. 11. (a) Block diagram of the proposed algebraic-based PWM modulation for the current source converters. (b) Three-phase non-symmetrical load with the four-leg current source inverter.

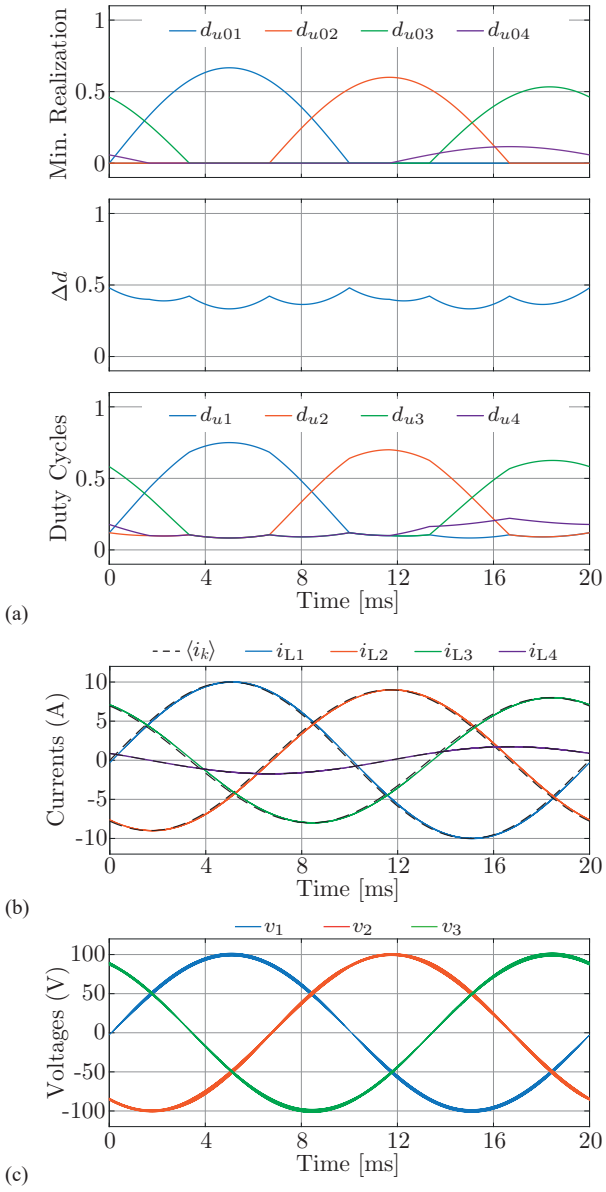


Fig. 12. (a) Minimal realization duty cycles, total excess duty cycle and applied duty cycles for the four-leg inverter. (b) Currents of the four-leg inverter. (c) Symmetric voltages over the non-symmetric load kept by the four-leg inverter.

VIII. Experimental Results

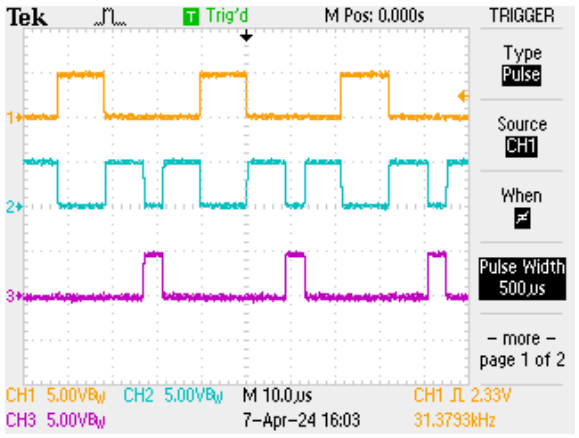
To provide experimental verification of the proposed concept on a three-phase current inverter example, a low power experimental setup is built using Arduino Uno R3 board [17] to provide pulse width modulated auxiliary waveforms s_{u1}, s_{u2}, s_{l1}, and s_{l2} according to Fig. 5, while additional logic circuitry is used to generate S_{u1}, S_{u2}, S_{u3}, S_{l1}, S_{l2}, and S_{l3}, according to the circuit diagram of Fig. 7, consisting of one CD4049 and one CD4081 circuit only. Using appropriate board configuration, the pulse width modulator frequency is set to 31.37 kHz. For the upper switches, pulse width waveforms at Arduino Uno pins 3 and 10 were used, since they share the same carrier waveform, while for the lower switches outputs at pins 9 and 11 were used for the same reason. Modulators for the upper and the lower switches both have triangular carriers corresponding to $\alpha = 0.5$, but they are not mutually synchronized. This causes the waveforms of Fig. 13(a) and (b) to be different than corresponding waveforms in Fig. 5, consisting of two patterns mirrored over time variable, each corresponding to one half of the switching period, glued one to another to cover the whole switching period.

In recording the waveforms, Tektronix TPS 2024 oscilloscope is used, and the experimental results rely on its ability to present average waveforms obtained over 128 recorded frames, as well as the capacity to measure four independent voltage waveforms, without the common ground. The averaging is used to provide duty ratio waveforms as they depend on time, since they are proportional to the average value of the pulse width modulated voltage over a switching period. Isolated probes are used to provide analog computation of generated currents according to (1), along with the averaging acquisition mode.

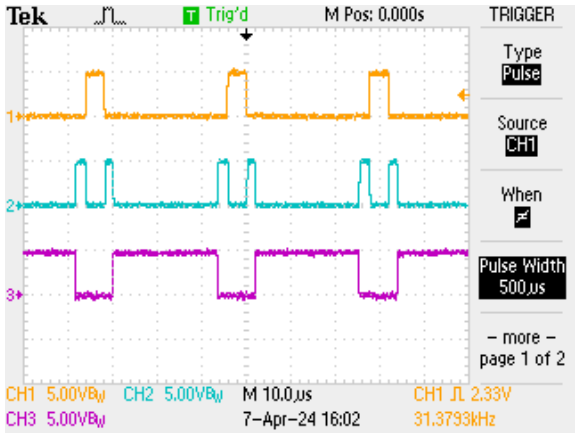
Three experimental examples are presented here, one with programming DC currents, one with programming symmetrical three-phase current set, and one that covers programming of arbitrary waveforms.

A. Programming of DC currents

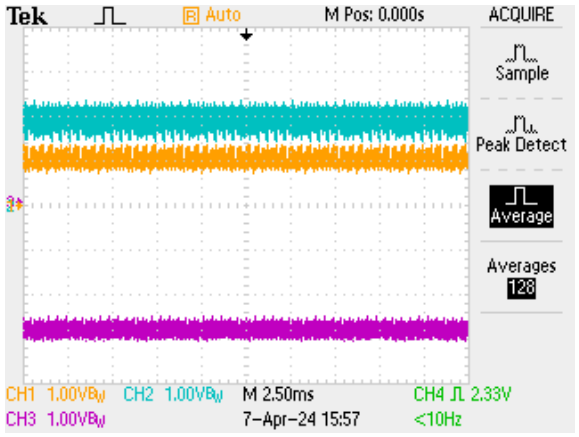
The first example covers a case of programming DC currents $i_1 = 1\,\text{A}$, $i_2 = 2\,\text{A}$, and $i_3 = -3\,\text{A}$, out of a DC-link current $I_{dc} = 5\,\text{A}$, resulting in $d_{u1} = 0.3333$, $d_{u2} = 0.5333$,



(a)

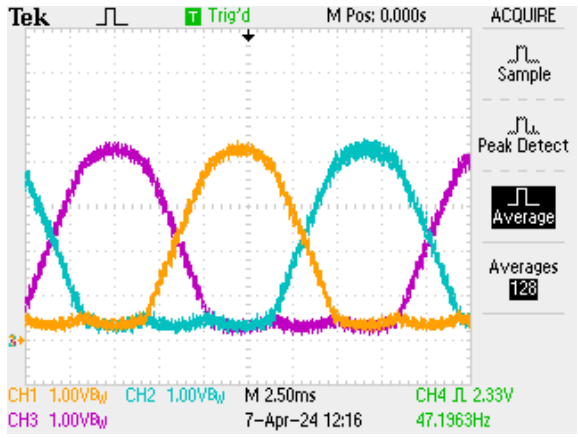


(b)

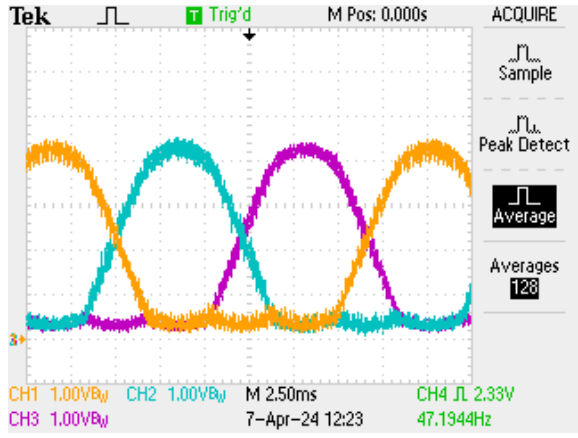


(c)

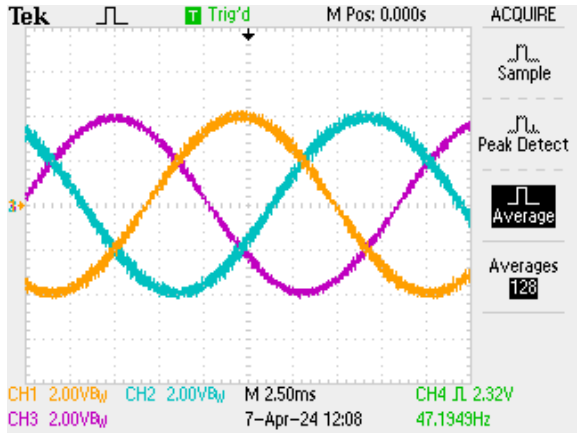
Fig. 13. Programming DC currents: (a) S_{uk}; (b) S_{lk}; (c) programmed currents, 1 A/div.



(a)



(b)



(c)

Fig. 14. Programming symmetrical AC currents: (a) d_{uk}; (b) d_{lk}; (c) programmed currents, 2 A/div.

$d_{u3} = 0.1333$, $d_{l1} = 0.1333$, $d_{l2} = 0.1333$, and $d_{l3} = 0.7333$. In Fig. 13(a) gating signal waveforms of the upper switches are presented, while in Fig. 13(b) gating signals of the lower switches are given. In both cases, it is clear that the switches conduct in a sequence, taking conduction one from another, providing continuous flow of the DC-link current. Obtained duty ratio values would provide currents shown in Fig. 13(c) that meet the required values.

B. Programming of symmetrical AC currents

As the second example, programming of currents $i_1 = 4\,\mathrm{A}\cos(\omega_0 t)$, $i_2 = 4\,\mathrm{A}\cos\left(\omega_0 t - \frac{2\pi}{3}\right)$, and $i_3 = 4\,\mathrm{A}\cos\left(\omega_0 t - \frac{4\pi}{3}\right)$ out of $I_{dc} = 5\,\mathrm{A}$ is considered, corresponding to $m = 0.8$. The programmed current system is symmetrical, and duty ratio waveforms for the upper switches are given in Fig. 14(a), while duty ratio values for the lower switches are shown in Fig. 14(b). Scale for the duty ratio values corresponds to $0.2\,(1/\mathrm{div})$, since the duty ratio values are generated averaging the pulse width modulated waveform that takes values 0 and 5 V, and actual scale for the averaged voltage is $1\,\mathrm{V/div}$. The waveforms correspond to the shapes given in Fig. 4 for $n = 3$. Result of applying such duty ratio values are generated currents presented in Fig. 14(c) that meet the required values.

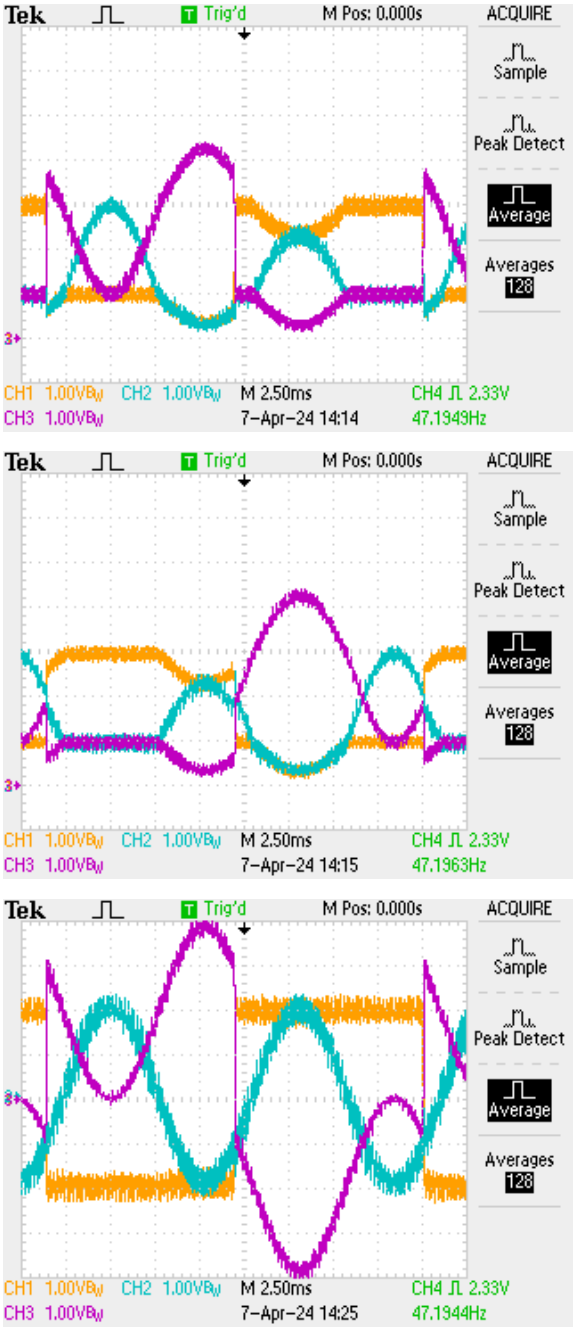


Fig. 15. Programming arbitrary waveforms: (a) d_{uk}; (b) d_{lk}; (c) programmed currents, 1 A/div.

C. Programming of arbitrary current waveforms

The last experimental example presented here covers programming of arbitrary current waveforms, in actual case currents $i_1 = 2\,\mathrm{A}\ \mathrm{sgn}\left(\cos\left(\omega_0 t\right)\right)$, $i_2 = 2\,\mathrm{A}\ \cos\left(2\,\omega_0 t - \frac{2\,\pi}{3}\right)$, and $i_3 = -i_1 - i_2$ are programmed out of $I_{dc} = 5\,\mathrm{A}$ according to the algorithm presented in Section III. Since the feasibility constraint (26) is met, adequate waveforms of duty ratio values could be computed, which are for the upper switches presented in Fig. 15(a), while for the lower switches in Fig. 15(b). The waveforms are rather unfamiliar to common practice, the same as the chosen set of currents to be programmed is, and the choice to present them is made just to illustrate what the proposed method can do with ease. Shown duty ratio values result in the current waveforms presented in Fig. 15(c), that match the required values.

IX. Conclusions

In this paper, pulse width modulation in general n-phase current source inverters is analyzed in its low-frequency part, below the switching frequency, where high-frequency effects are averaged out on the level of the switching period. Unknown $2\,n$ duty ratio values d_{uk} and d_{lk} for $k \in \{1, \ldots n\}$ are derived in the general case of arbitrary waveforms of the inverter output currents first. The analysis resulted in a conclusion that the duty ratio functions are not unique and that there are $n-1$ degrees of freedom, though within a boundary that limits their sum. This can be used to optimize the inverter performance according to an optimization criterion. The method does not rely on space vector representation but is solely based on linear algebra.

A special case of a symmetrical polyphase current system is analyzed next, and the duty ratio values are derived as functions of time. It is shown that there is a limit on the generated current amplitude, which depends on the number of phases, equal to the DC-link current only in two-phase and three-phase systems. The method is generalized to arbitrary periodic waveforms of generated currents next to determine the maximal amplitude and provide the waveform scaling in this generalized case.

A pulse width modulator that implements introduced method is proposed, consisting of two parts, for the upper switches and for the lower switches, and requiring simple components only.

The technique is verified by simulation using standard simulation tools first. Next, the modulator prototype is built using Arduino Uno board and some additional logic circuitry, completely verifying the proposed methods, and illustrating both the method and the modulator in cases of programming three DC currents, a symmetrical three-phase current system, and three arbitrary current waveforms.

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