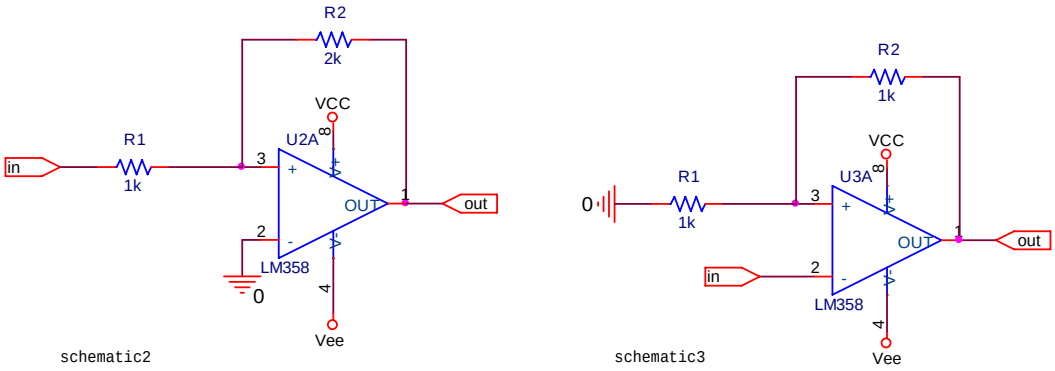
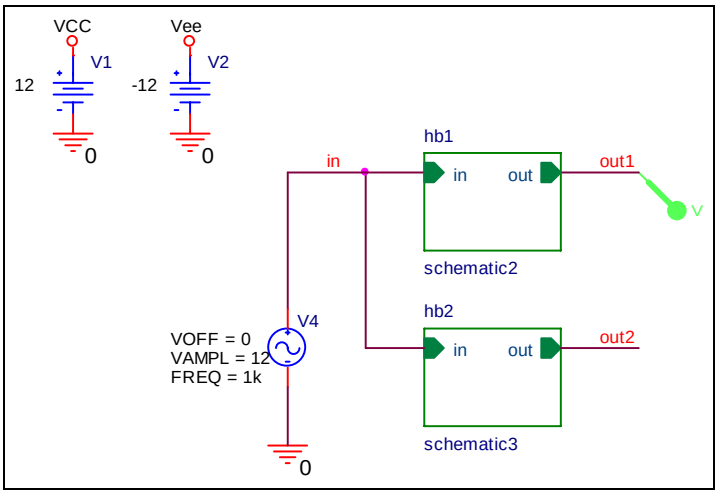
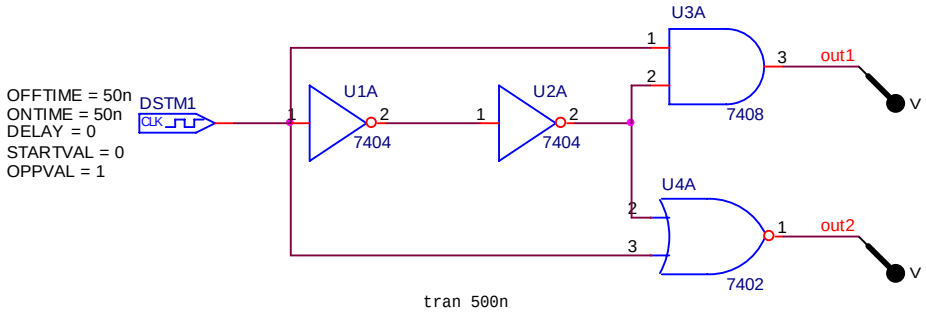


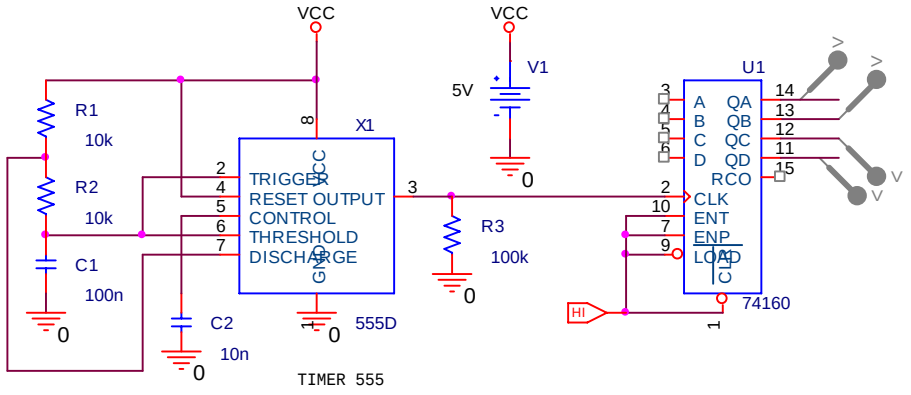


schematic1

Kreiranje šeme za simulaciju pomoću hijerarhijskih blokova



Simulacija digitalnih kola i uočavanje kašnjenja



Timer 555 i binarni brojac: Tran 40m (+7442a)