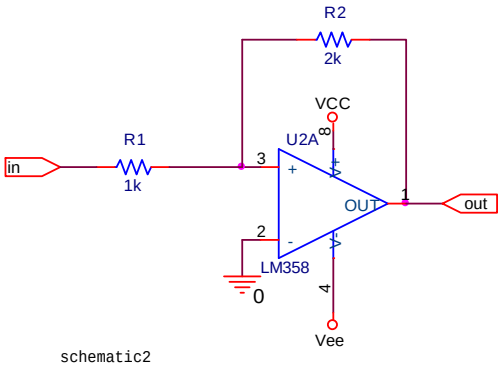
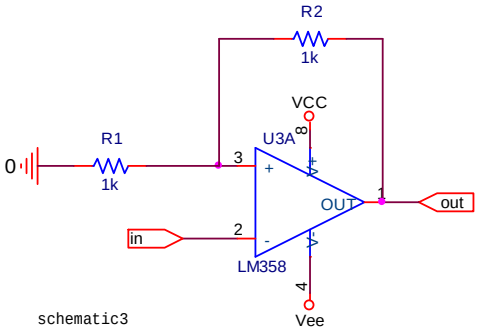
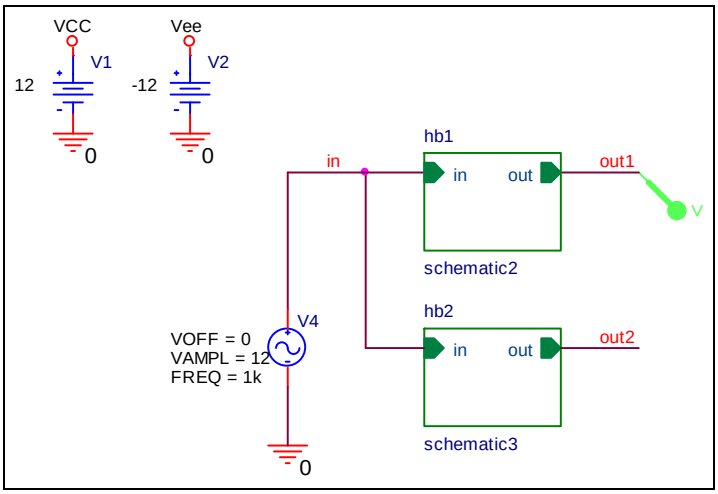
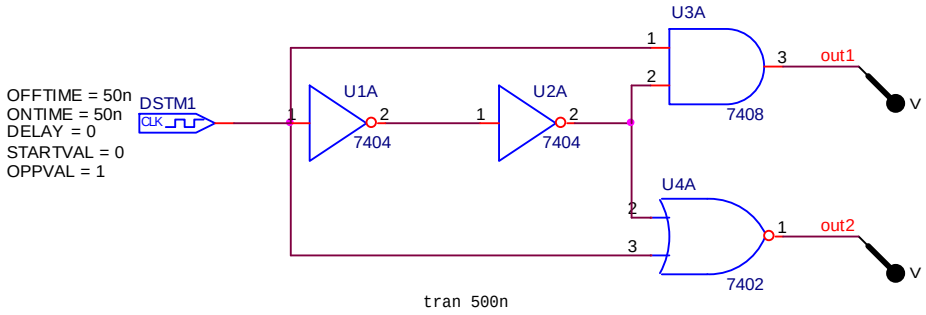




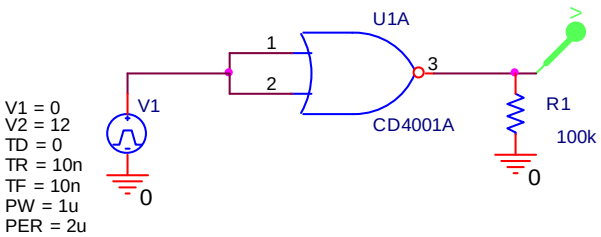


schematic1

Kreiranje šeme za simulaciju pomoću hijerarhijskih blokova



Simulacija digitalnih kola i uočavanje kašnjenja



Promena napona napajanja logickih kola