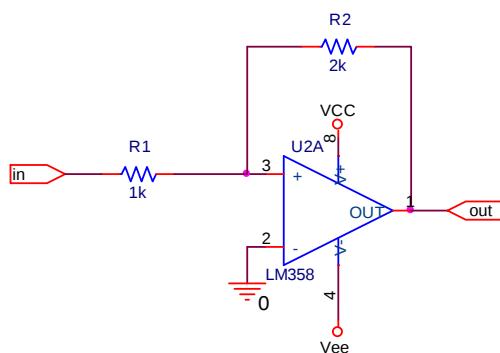
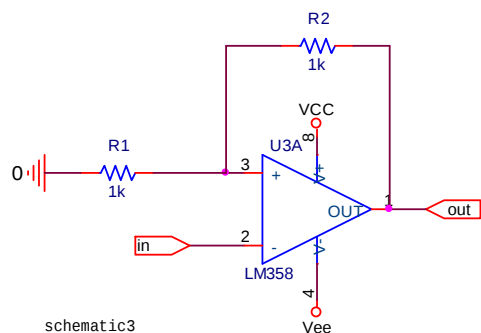
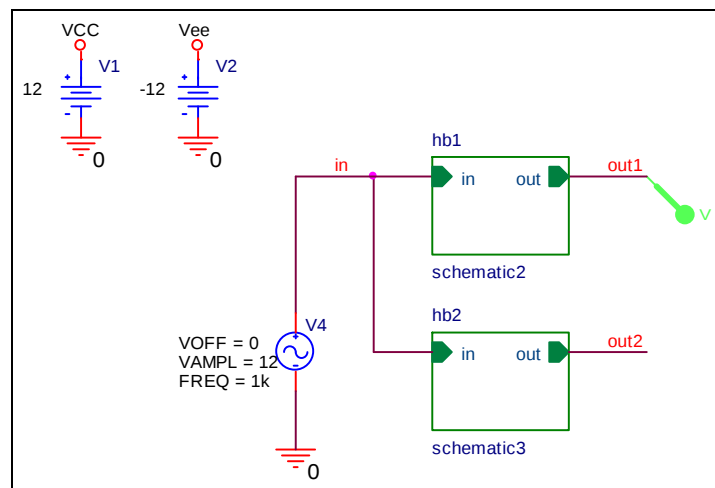




schematic2

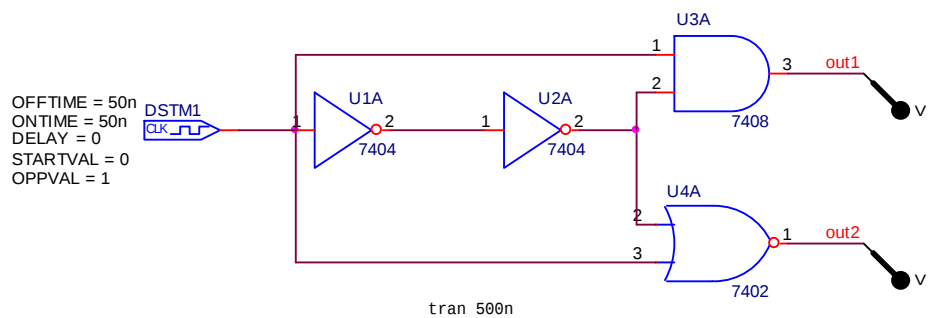


schematic3



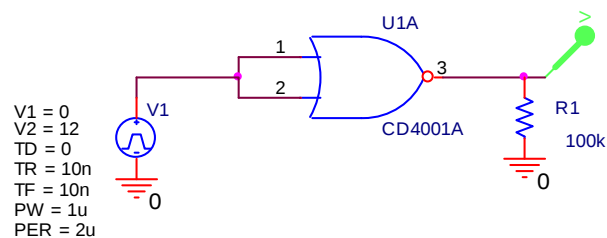
schematic1

Kreiranje šeme za simulaciju pomoću hijerarhijskih blokova



tran 500n

Simulacija digitalnih kola i uočavanje kašnjenja



PARAMETERS:
cd4000_vdd = 12

Promena napona napajanja logickih kola