PhD Position Opening
at UPM's Information Processing and Telecommunication Center

Advanced Circuits and Methods for Heterogeneous Integration

SCOPE

Microelectronics based on silicon CMOS technology has reached extraordinary levels of integration and complexity, while achieving high levels of manufacturing maturity, especially for digital designs. The continuous improvement of high-density circuits driven by Moore's Law has led to System-on-Chip (SoC) architectures, that integrate more and more functionality onto a single chip. However, the larger size of integrated circuits increases the likelihood of manufacturing defects, resulting in lower performance and significant higher costs. In response to these challenges, the industry is turning to **advanced integration and packaging** technologies to keep pace with rising processing capabilities.

Recent advances in certain technologies have made ***chiplets*** a viable and effective option to help combat the slowdown of Moore's Law. The idea is to divide a complex SoC into multiple smaller chiplets which can provide a potentially more cost-effective and scalable solution. To achieve the functionality and performance of a monolithic SoC, it is critical to have integration technologies that enable high-speed communication between chiplets, even on different technologies. Therefore, there is a clear opportunity for heterogeneous integration and system-level scaling.

Additionally, advanced radio frequency (RF) systems, such as 5G-6G wireless communications and automotive radar, use the microwave and millimeter bands (3 GHz-300 GHz) as a means of communication and sensing, placing serious demands on their electronic circuits, with technologies other than silicon. The proposed PhD thesis will contribute to the progress in the design of RF and mixed-signal integrated circuits for their **heterointegration** into a complex electronic system.

REQUIREMENTS

- A master's degree in Electronic Engineering, Telecommunication Engineering, or similar degrees
- Experience in design tools (Cadence, Synopsys, ADE) is highly desirable.
- Computational skills are valuable.
- Good academic record
- Great motivation for scientific work and ability for teamwork
- Full proficiency in English.
- Starting date in Q2 2024.

GENERAL CONDITIONS

- The selected candidate would start her/his PhD in our group, hired from a research project in the context of the UPM-Indra Chair (industrial PhD) with an expected duration of 3 to 4 years.
- Excellent experimental infrastructure and international atmosphere.
- Attendance to scientific conferences worldwide
- Research stays in partner labs in Europe, Japan or the USA

APPLICATIONS

Interested candidates should send a motivation letter, his/her CV and transcripts of all undergraduate and graduate coursework to Prof. Marisa Lopez-Vallejo (**m.lopez.vallejo@upm.es**) or Prof. Ruzica Jevtic (**r.jevtic@upm.es**).

March 2024