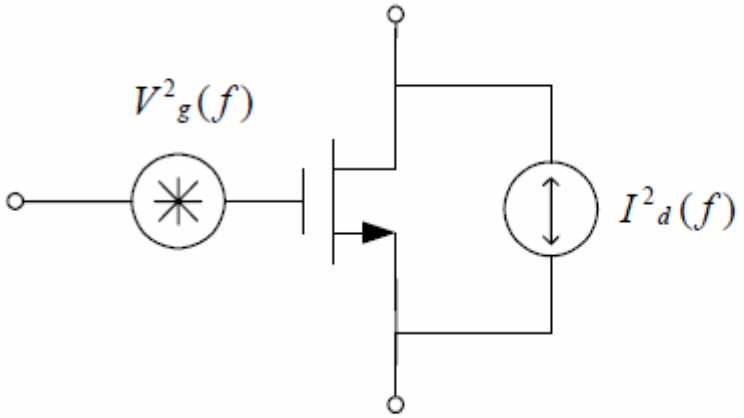
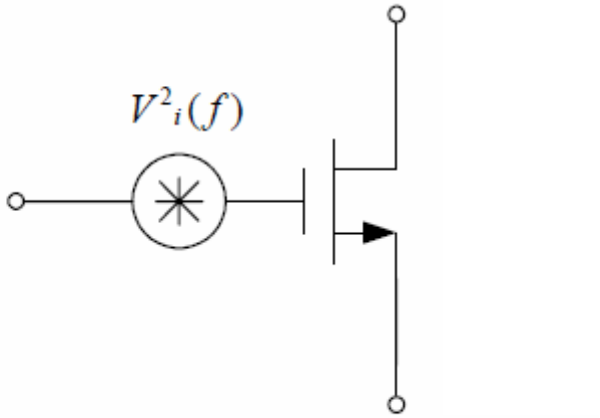
# Low noise OTA

## Noise Models for MOSFETs:

•The dominant noise sources for active MOSFET transistors are flicker and thermal noise
•Simplified model for low and moderate frequencies




$$V^2_g(f) = \frac{K}{WLC_{ox}f} \qquad I^2_d(f) = 4kT\left(\frac{2}{3}\right)g_m \qquad V^2_i(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K}{WLC_{ox}f}$$

•Note that the 1/f noise is inversely proportional to the transistor area, WL. 1/f noise is extremely important in MOSFET circuits, because it dominates at low frequencies unless some switching-techniques are used to reduce its effect.
•This noise is related with the majority carriers being trapped by the electron energy states close to the Si-SiO2 interface. It relates to the contamination and crystal defects in the semiconductor material.
•Typically, p-channel transistors have less flicker noise than their n-channel counterparts since their majority carriers (holes) are less likely to be trapped due to their lower mobility.
•The name 1/f comes from the fact that the flicker noise power spectral density decreases almost linearly with increasing frequency.

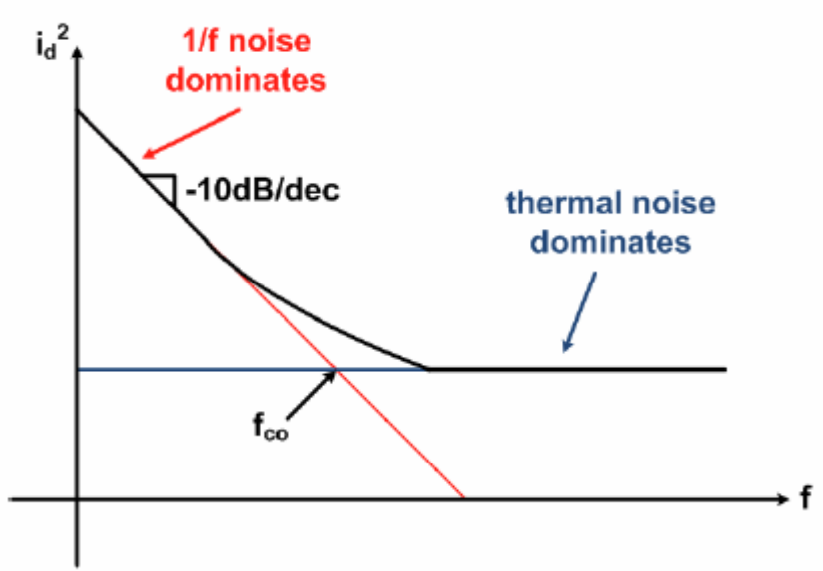
•The thermal noise in a MOSFET is due to the resistive channel in the active region.
•If the transistor was in triode region, the thermal noise current in the drain would simply be given by Id^2(f) = 4kT/rds , where rds is the channel resistance.
•When the transistor is in the active region, the channel cannot be considered homogeneous. Therefore, the total noise is found by integrating over small portions of the channel. Such an integration results in the noise current in the drain being given by

$$I_d^2(f) = 4kT\gamma g_m,\ I_{dLCH}^2(f) = 4kT\frac{2}{3}g_m,\ 0.8 \le \gamma_{SCH} \le 1$$

•1/f Noise Corner Frequency: This is the frequency at which the flicker noise density equals the thermal noise density

$$\frac{K_F g_m^2}{WLC_{ox}f_{co}} = 4kT\gamma g_m$$

$$f_{co} = \frac{K_F}{4kT\gamma C_{ox}}\frac{g_m}{WL} = \frac{K_F}{4kT\gamma C_{ox}}\frac{1}{L}\left(\frac{g_m}{I_D}\right)\left(\frac{I_D}{W}\right)$$

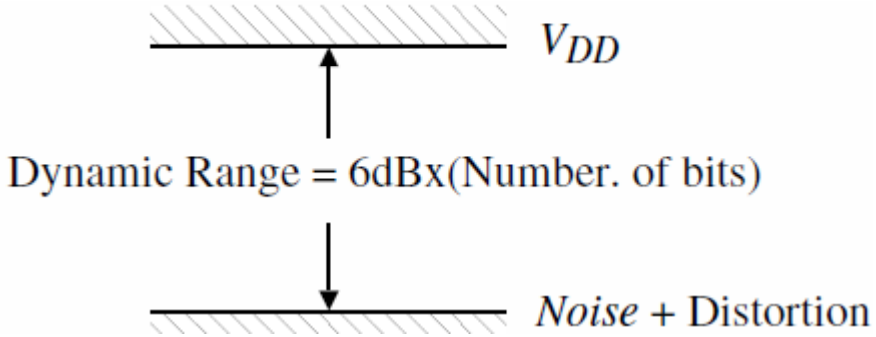



•For a given gm/ID (which sets ID/W), the only way to reduce fco is to use longer channel devices

## ➢Minimization of Noise in Op Amps

•Why do we need low noise op amps?
•Dynamic range:
•Signal-to-noise ratio

$$SNR = \frac{\max RMS \text{ signal}}{\text{Noise}}$$




•Consider a 14 bit digital-to-analog converter with a 1V reference with a bandwidth of 1MHz.

Maximum RMS signal is 0.5V/√2=353.5mVrms
A 14 bit D/A converter requires 14x6dB dynamic range or 84 dB or 16400.
The value of the least significant bit (*LSB)* is 0.3535/16400=21.6μVrms
If the equivalent input noise of the op amp is not less than this value, then the LSB cannot be resolved and the D/A converter will be in error. An op amp with an equivalent input-noise spectral density of 10nV/ Hz will have an rms noise voltage of approximately (10nV/ Hz)(1000 Hz) = 10μVrms in a 1MHz bandwidth.

**Minimization of Noise in CMOS Op Amps**

1) Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)
2) To minimize the 1/f noise:
   a) Use PMOS input transistors with appropriately selected dc currents and W and L values.
   b) Use lateral BJTs to eliminate the 1/f noise.
   c) Use chopper stabilization to reduce the low-frequency noise.

**Noise Analysis**

1) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

2) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

3) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.

## ▪A Low-Noise, Two-Stage, Miller Op Amp

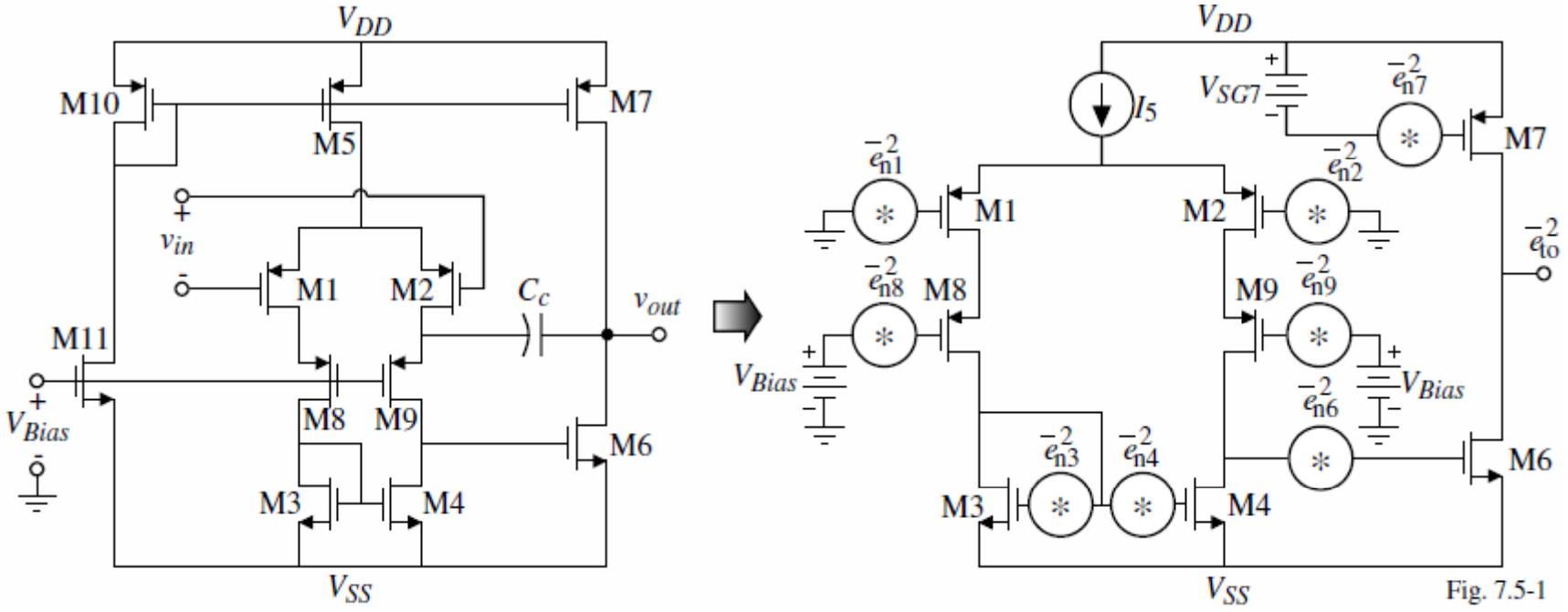


Fig. 7.5-1

•PMOS device are selected for the input of the differential stage because of their lower 1/f noise

•We have ignored the noise contributed by M5.

$$g_{m9eff} = \frac{g_{m9}}{1+g_{m8}r_{ds2}} \approx \frac{1}{r_{ds2}}$$

$$g_{m8eff} = \frac{g_{m8}}{1+g_{m8}r_{ds1}} \approx \frac{1}{r_{ds1}}$$

$$e_{n1}^2 = e_{n2}^2, e_{n3}^2 = e_{n4}^2, e_{n6}^2 = e_{n7}^2, e_{n8}^2 = e_{n9}^2$$

$$A_v = g_{m1}R_I g_{m6}R_{II}$$

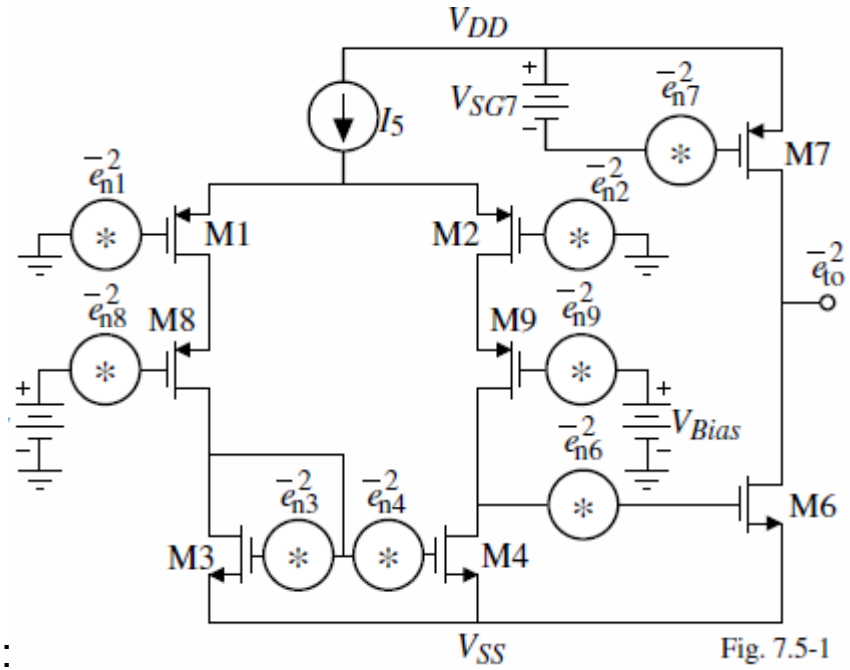


Fig. 7.5-1

•The total output voltage noise spectral density is:

$$e_{to}^2 = \left(g_{m6}R_{II}\right)^2\left[e_{n6}^2 + e_{n7}^2 + R_I^2\left(g_{m1}^2e_{n1}^2 + g_{m2}^2e_{n2}^2 + g_{m3}^2e_{n3}^2 + g_{m4}^2e_{n4}^2 + \frac{e_{n8}^2}{r_{ds1}^2} + \frac{e_{n9}^2}{r_{ds2}^2}\right)\right]$$

•The equivalent input voltage noise spectral density is:

$$e_{eq}^2 = \frac{e_{to}^2}{A_v^2} = \frac{e_{to}^2}{\left(g_{m1}R_I g_{m6}R_{II}\right)^2} = \frac{2e_{n6}^2}{\left(g_{m1}R_I\right)^2} + 2e_{n1}^2\left(1+\left(\frac{g_{m3}}{g_{m1}}\right)^2\frac{e_{n3}^2}{e_{n1}^2} + \frac{1}{g_{m1}^2r_{ds1}^2}\frac{e_{n8}^2}{e_{n1}^2}\right)$$

$$e_{eq}^2 \approx 2e_{n1}^2\left(1+\left(\frac{g_{m3}}{g_{m1}}\right)^2\frac{e_{n3}^2}{e_{n1}^2}\right)$$

## •1/*f* Noise of a Two-Stage, Miller Op Amp

$$e_{ni}^2 = \frac{B}{fW_iL_i}\left[\mathrm{V}^2/\mathrm{Hz}\right]$$

$$e_{eq,1/f}^2 \approx 2e_{n1}^2\left(1+\left(\frac{k_n}{k_p}\frac{B_N}{B_P}\right)^2\left(\frac{L_1}{L_3}\right)^2\right)$$

•Because we have selected PMOS input transistors, en1 has been minimized if we choose $W_1L_1$ ($W_2L_2$) large.
•Make L1<<L3 to remove the influence of the second term in the brackets.

## •Thermal Noise of a Two-Stage, Miller Op Amp

$$e_{ni}^2 = \frac{8kT}{3g_{mi}}\left[\mathrm{V}^2/\mathrm{Hz}\right]$$

$$e_{eq,T}^2 \approx 2e_{n1}^2\left(1+\sqrt{\frac{k_n}{k_p}\frac{W_3}{W_1}\frac{L_1}{L_3}}\right)$$

•The choices that reduce the 1/f noise also reduce the thermal noise
•Noise Corner:

$$f_c = \frac{3g_mB}{8kTWL}$$

## Example: Design of A Two-Stage, Miller Op Amp for Low 1/f Noise

Use the model parameters of *Kn = 120μA/V2, Kp= 25μA/V^2, and Cox = 6fF/μm^2* along with the value of *KF = 4x10-28 F·A* for NMOS and *0.5x10-28 F·A* for PMOS and design the previous op amp with *ID5 = 100μA* to minimize the 1/f noise. Calculate the corresponding thermal noise and solve for the noise corner frequency. From this information, estimate the rms noise in a frequency range of 1Hz to 100kHz. What is the dynamic range of this op amp if the maximum signal is a 1V peak-to-peak sinusoid?

*Solution:*

1) The 1/f noise constants, $B_N$ and $B_P$ are calculated as follows

$$B_N = \frac{KF}{2C_{ox}K_n} = 1.33\cdot 10^{-22}\left(\mathrm{Vm}\right)^2 \qquad B_P = \frac{KF}{2C_{ox}K_p} = 1.67\cdot 10^{-22}\left(\mathrm{Vm}\right)^2$$

2) Now select the geometry of the various transistors that influence the noise performance.
   - To keep $e_{n1}$ small, let $W_1$ = 100μm and $L_1$ = 1μm. Select $W_3$ = 10μm and $L_3$ = 20μm and let $W_8$ and $L_8$ be the same as $W_1$ and $L_1$ since they little influence on the noise.
   - $M_1$ is matched with $M_2$, $M_3$ with $M_4$, and $M_8$ with $M_9$

$$e_{n1,1/f}^2 = \frac{B_P}{fW_1L_1} = \frac{1.67\cdot 10^{-12}}{f}\left(\mathrm{V}^2/\mathrm{Hz}\right)$$

$$e_{eq,1/f}^2 \approx 2e_{n1}^2\left(1+\left(\frac{k_n}{k_p}\frac{B_N}{B_P}\right)^2\left(\frac{L_1}{L_3}\right)^2\right) = 2\frac{1.67\cdot 10^{-12}}{f}\left(1+\left(\frac{120}{25}\frac{1.33}{1.67}\right)^2\left(\frac{1}{20}\right)^2\right)\left(\mathrm{V}^2/\mathrm{Hz}\right) = \frac{3.452\cdot 10^{-12}}{f}\left(\mathrm{V}^2/\mathrm{Hz}\right)$$

- Note at 100Hz, the voltage noise in a 1Hz band is ≈ 3.45x10^(-14)V^2(rms) or 0.186μV(rms).

3) The thermal noise at room temperature is

$$e_{n1}^2 = \frac{8kT}{3g_{m1}}\left(\mathrm{V}^2/\mathrm{Hz}\right) = 2.208\cdot 10^{-17}\left(\mathrm{V}^2/\mathrm{Hz}\right)$$

$$e_{eq,T}^2 \approx 2e_{n1}^2\left(1+\sqrt{\frac{k_n}{k_p}\frac{W_3}{W_1}\frac{L_1}{L_3}}\right) = 2\cdot 2.208\cdot 10^{-17}\left(1+\sqrt{\frac{120}{25}\frac{10}{100}\frac{1}{20}}\right)\left(\mathrm{V}^2/\mathrm{Hz}\right) = 5.093\cdot 10^{-17}\left(\mathrm{V}^2/\mathrm{Hz}\right)$$

4) The noise corner frequency is found by equating the two expressions for $e_{eq}$ to get

$$f_c = \frac{3.452\cdot 10^{-12}}{5.093\cdot 10^{-17}} = 67.8\ \mathrm{kHz}$$

•This noise corner is indicative of the fact that the thermal noise is much less than the 1/f noise.

5) To estimate the rms noise in the bandwidth from 1Hz to 100kHz, we will ignore the thermal noise and consider only the 1/f noise. Performing the integration gives

$$V_{eq,rms}^2 = \int_1^{10^5} \frac{3.452\cdot 10^{-12}}{f} df = 3.452\cdot 10^{-12}\left[\ln\left(10^5\right)-\ln(1)\right] = 0.408\cdot 10^{-10}\,\mathrm{V}^2$$

$$\Rightarrow V_{eq,rms} = 6.39\,\mu\mathrm{V}$$

•The maximum signal in rms is 0.353V. Dividing this by 6.39μV gives 55,279 or 94.85dB which is equivalent to more than 15 bits of resolution.

6) Note that the design of the remainder of the op amp will have little influence on the noise and is not included in this example.

## ▪Low-Noise Op Amp using Lateral BJT's at the Input

**Lateral BJT**

•Since the 1/f noise is associated with current flowing at the surface of the channel, the lateral BJT offers a lower 1/f noise input device because the majority of current flows beneath the surface.

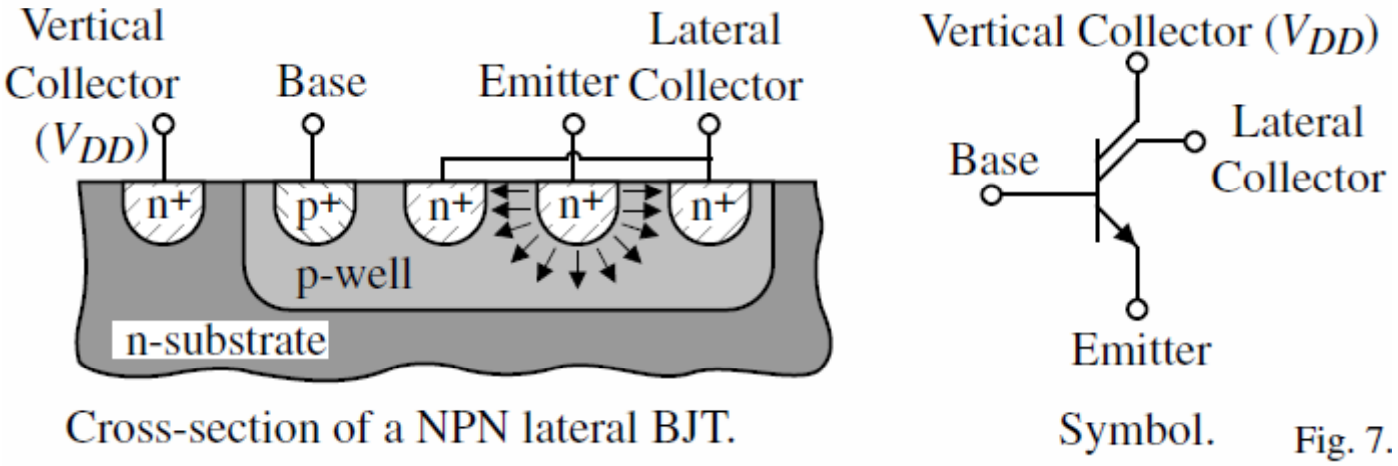



Fig. 7.

Comments:

• Base of the BJT is the well

• Two collectors-one horizontal (desired) and one vertical (undesired)

• Collector efficiency is defined as Lateral collector current/Total collector current and is 60-70%

• Reverse biased collector-base acts like a photodetector and is often used for light sensing purposes

## Physical Layout of a Lateral PNP Transistor

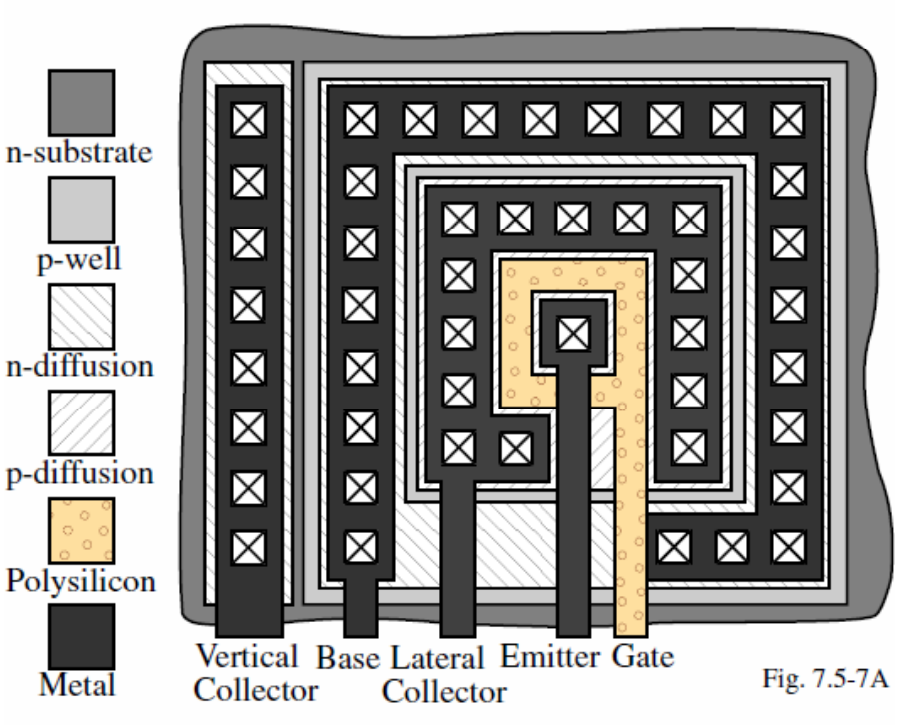



Fig. 7.5-7A

•Generally, the above structure is made as small as possible and then paralleled with identical geometries to achieve the desired BJT.

•Experimental Results for a x40 PNP lateral BJT:

| Characteristic | Value |
|---|---|
| Transistor area | $0.006\text{mm}^2$ |
| Lateral $\beta$ | 90 |
| Lateral efficiency | 70% |
| Base resistance | 150Ω |
| $e_n$ at 5 Hz | $2.46\text{nV}/\sqrt{\text{Hz}}$ |
| $e_n$ at midband | $1.92\text{nV}/\sqrt{\text{Hz}}$ |
| $f_c(e_n)$ | 3.2Hz |
| $i_n$ at 5 Hz | $3.53\text{pA}/\sqrt{\text{Hz}}$ |
| $i_n$ at midband | $0.61\text{pA}/\sqrt{\text{Hz}}$ |
| $f_c(i_n)$ | 162 Hz |
| $f_T$ | 85 MHz |
| Early voltage | 16V |
| 1.2μm CMOS with n-well | |

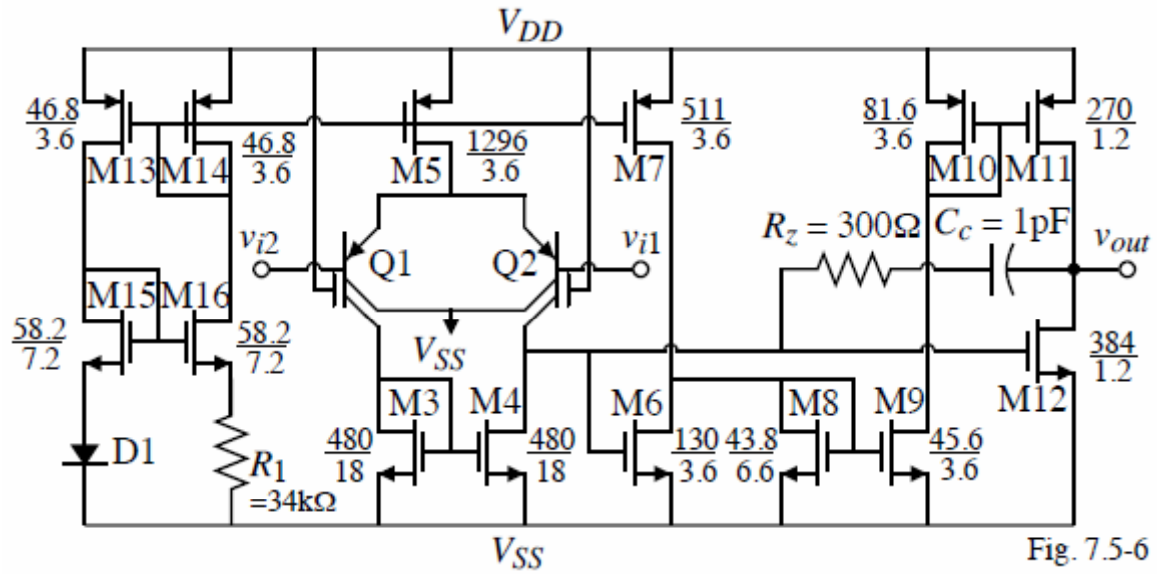
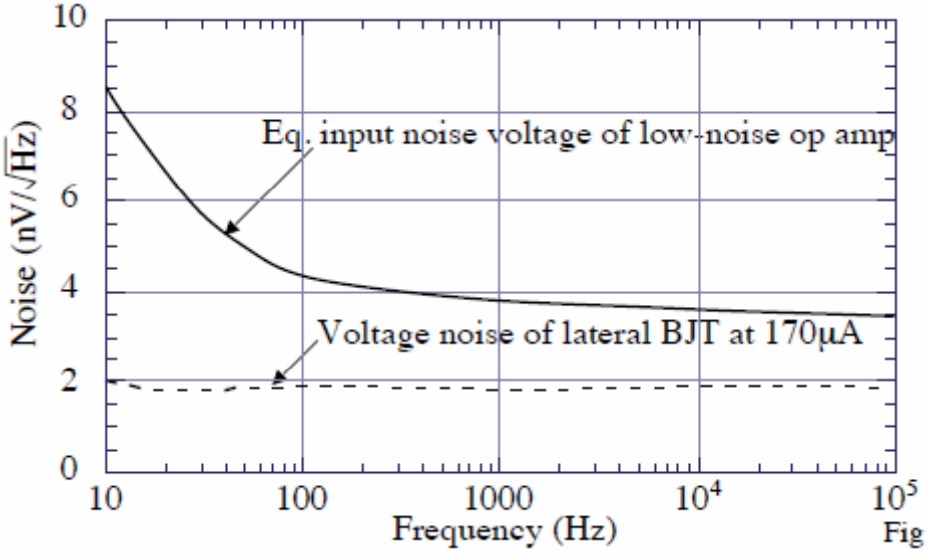


Fig. 7.5-6

•Experimental noise performance:



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